



AL4V8M440x2 Data Sheet

Vision V1.0

Preliminary Version

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Amendments

04-11-03 Preliminary Version

AL4V8M440x2 8M-Bits Dual Module FIFO Field Memory

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1.0 Description

The AL4V8M440x2 has dual 512K x 8 FIFO modules embedded in a single chip package. Each module in the chip is operated individually as if a stand alone 512K x 8 FIFO. The AL4V8M440x2 FIFO memory provide completely independent 8-bit input and output ports that allow read and write data from FIFO simultaneously. The built-in address and pointer control circuits provide a straightforward bus interface to serially read/write memory that can reduce inter-chip design efforts. Manufactured using a state-of-the-art embedded high density memory cell array. The AL4V8M440x2 use high performance process technologies with extended controller functions (write mask, read skip, selectable polarity ... etc.); allow easy operation of non-linearity FIFO read/write for Digital TV, security system and video camera applications.

The 8M-bits of AL4V8M440x2 are configured as dual 512K x 8-bit FIFO to accommodate NTSC, PAL or up to SVGA resolution. Running at high speed (50 MHz maximum) and low power consumption AC characteristics (3.3V power supply) allow the high performance and high quality application capability.

The FIFO can sequentially queue in data at rising edge of write clock when write enable is activated. Likewise, the FIFO can sequentially output data at rising edge of read clock when both read enable and output enable are activated.

Additional manipulation is produced by the Input and Output Enable control signals. The application can use input enable to control whether new data is going to be written over the old data or not. For read data, the output enable signal can control whether data is going to be skipped during the read operation. To have better control flexibilities in the inter-chip design, the polarities of the AL440B control signals are selectable. The read and write ports control signals, such as Read/Write Enable, Input/Output Enable., can be either active low or high by pulling /PLRTY signal to high or low respectively. The AL4V8M440x2 can still keep the data not evaporating without an external running clock during power saving mode.

These chips are available as an 80-pin TQFP package supporting dual 8-bit FIFO modules; the small footprint allows product designers to keep real estate to a minimum.

2.0 Features

- 8Mbit (dual 512kx 8) organization FIFO
- Queues Video Chroma and Luma data by separating memory cells in single package
- Supports NTSC, PAL and HDTV (512kx 8 can do up to SVGA resolution)
- Independent 8bit read/write port operations (different read/write data rates acceptable)
- Read/Write Clock Speed: 50 Mhz
- Cascade supports (for one field delay)
- Input Enable (write mask) / Output Enable (data skipping) control
- Selectable control signal polarity
- Self refresh
- 3.3V power supply with 5V signal input tolerance
- Standard 80-pin TQFP package

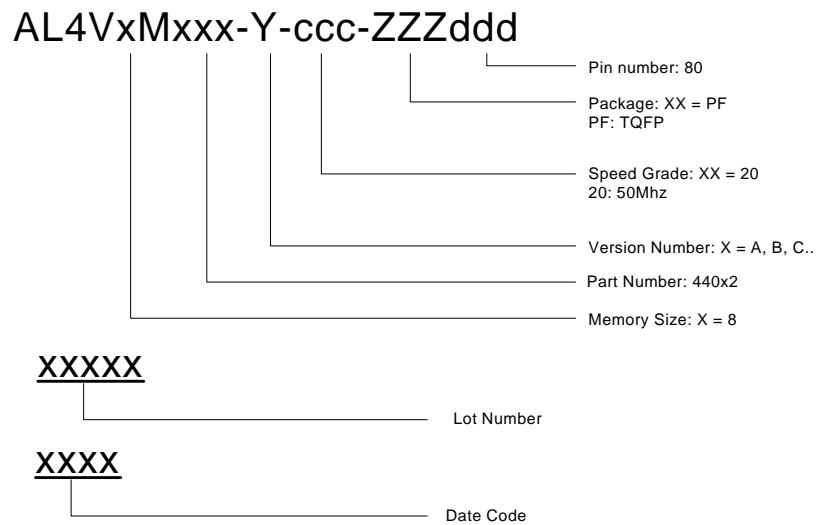
3.0 Applications

- Multimedia systems
- Video capture or editing systems for NTSC/PAL or SVGA resolution
- Security systems
- Scan rate converters
- TBC (Time Base Correction)
- Frame synchronizer
- Digital video camera
- Hard disk cache memory
- Buffer for communication systems

4.0 Ordering Information

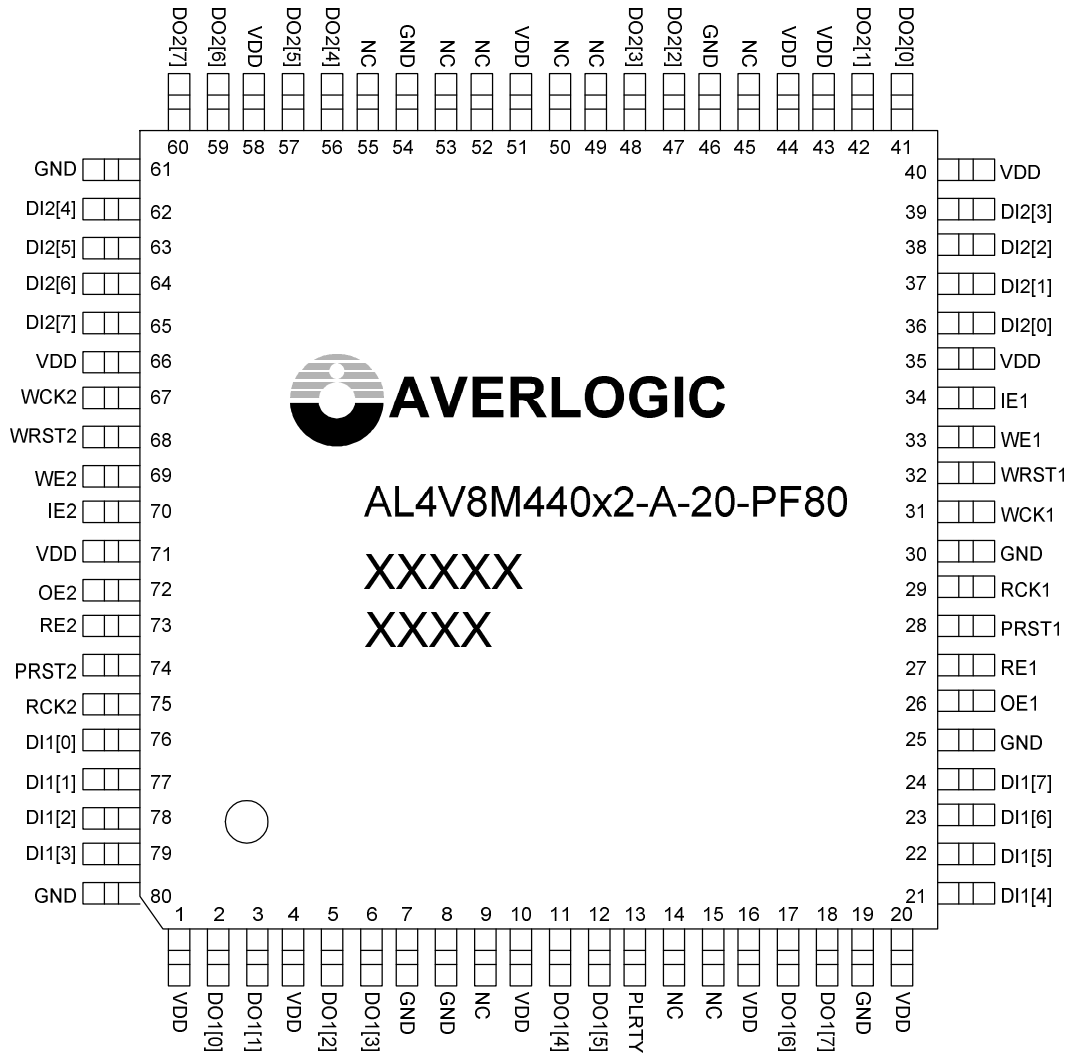
| Part number | Package | Power Supply | Status |
|------------------------|---------------------------|--------------|--------|
| AL4V8M440x2-20 (50MHz) | PF80: 80-pin plastic TQFP | +3.3 volt | 2004 |

4.1 Marking Information



5.0 Pin-out Diagram

The AL4V8M440x2 pin-out diagram is following.



TQFP - 80 PACKAGE TOP VIEW

6.0 Pin Definition and Description

The pin definitions and descriptions are as follows:

Write Bus Signals

| Pin name | Pin number | I/O type | Description |
|----------|--------------|----------|---|
| DI1[7:0] | 76~79, 21~24 | I | The DI1 pins input 8bits of data for port 1. Data input is synchronized with the WCK1 clock. Data is acquired at the rising edge of WCK1 clock. |

| | | | |
|----------|--------------|---|---|
| DI2[7:0] | 36~39, 62~65 | I | The DI2 pins input 8bits of data for port 2. Data input is synchronized with the WCK2 clock. Data is acquired at the rising edge of WCK2 clock. |
| WE1 | 33 | I | WE1 is an input signal that controls the 8bit input data write and write pointer operation for port 1. |
| WE2 | 69 | I | WE2 is an input signal that controls the 8bit input data write and write pointer operation for port 2. |
| IE1 | 34 | I | IE1 is an input signal that controls the enabling/ disabling of the 8bit data input pins for port 1. The internal write address pointer is always incremented at rising edge of WCK1 by enabling WE1 regardless of the IE1 level. |
| IE2 | 70 | I | IE2 is an input signal that controls the enabling/ disabling of the 8bit data input pins for port 2. The internal write address pointer is always incremented at rising edge of WCK2 by enabling WE2 regardless of the IE2 level. |
| WCK1 | 31 | I | WCK1 is the write clock input pin for port 1. The write data input is synchronized with this clock. |
| WCK2 | 67 | I | WCK2 is the write clock input pin for port 2. The write data input is synchronized with this clock. |
| WRST1 | 32 | I | The WRST1 is a reset input signal that resets the write address pointer to 0 for port 1. |
| WRST2 | 68 | I | The WRST2 is a reset input signal that resets the write address pointer to 0 for port 2. |

*Note: For the polarity definition of all write control signals (WE1/WE2, IE1/IE2 and WRST1/WRST2), please refer to /PLRTY pin definition and “Memory Operation” section for details.

Read Bus Signals

| Pin name | Pin number | I/O type | Description |
|----------|----------------------------|----------|--|
| DO1[7:0] | 2~3, 5~6, 11~12, 17~18 | O | The DO1 pins output 8bit of data for port 1. Data output is synchronized with the RCK1 clock. Data is output at the rising edge of the RCK1 clock. |
| DO2[7:0] | 41~42, 47~48, 56~57, 59~60 | O | The DO2 pins output 8bit of data for port 2. Data output is synchronized with the RCK2 clock. Data is output at the rising edge of the RCK2 clock. |
| RE1 | 27 | I | RE1 is an input signal that controls the 8bit output data |

| | | | |
|-------|----|---|---|
| | | | read and read pointer operation for port 1. |
| RE2 | 73 | I | RE is an input signal that controls the 8bit output data read and read pointer operation for port 2. |
| OE1 | 26 | I | OE1 is an input signal that controls the enabling/ disabling of the 8bit data output pins for port 1. The internal read address pointer is always incremented at rising edge of RCK1 by enabling RE1 regardless of the OE1 level. |
| OE2 | 72 | I | OE2 is an input signal that controls the enabling/ disabling of the 8bit data output pins for port 2. The internal read address pointer is always incremented at rising edge of RCK2 by enabling RE2 regardless of the OE2 level. |
| RCK1 | 29 | I | RCK1 is the read clock input pin for port 1. The read data output is synchronized with this clock. |
| RCK2 | 75 | I | RCK2 is the read clock input pin for port 2. The read data output is synchronized with this clock. |
| RRST1 | 28 | I | The RRST1 is a reset input signal that resets the read address pointer to 0 for port 1. |
| RRST2 | 74 | I | The RRST2 is a reset input signal that resets the read address pointer to 0 for port 2. |

*Note: For the polarity definition of all read control signals (RE1/RE2, OE1/OE2 and RRST1/RRST2), please refer to /PLRTY pin definition and “Memory Operation” section for details.

Power/Ground Signals

| Pin name | Pin number | I/O type | Description |
|-----------------|---|----------|-------------|
| V _{DD} | 1,4, 10, 16, 20, 35, 40, 43, 44, 51, 58, 66, 71 | - | 3.3V ± 10%. |
| GND | 7, 8, 19, 25,30, 46, 54, 61, 80 | - | Ground. |

Miscellaneous Signals

| Pin name | Pin number | I/O type | Description |
|----------|------------|----------|---|
| /PLRTY | 13 | I | Select active polarity of the control signals including WE1/WE2, RE1/RE2, WRST1/WRST2, RRST1/RRST2, IE1/IE2 and OE1/OE2 totally 12 signals /PLRTY = V _{DD} , active low. /PLRTY = GND, active high. Note: during memory operation, the pin must be permanently connected to VDD or GND. If /PLRTY level |

| | | | |
|----|--------------------------------------|---|--|
| | | | is changed during memory operation, memory data is not guaranteed. |
| NC | 9, 14~15, 45, 49~50, 52~53, 55 | - | No connect or connect to Ground |

7.0 Electrical Characteristics

7.1 Absolute Maximum Ratings

| Parameter | | Rating | Unit |
|------------------|-------------------------|--------------------------------|------|
| V _{DD} | Supply Voltage | -0.3 ~ +3.8 | V |
| V _P | Pin Voltage | -0.3 ~ +(V _{DD} +0.3) | V |
| I _O | Output Current | -20 ~ +20 | mA |
| T _{AMB} | Ambient Op. Temperature | 0 ~ +85 | °C |
| T _{stg} | Storage temperature | -40 ~ +125 | °C |

7.2 Recommended Operating Conditions

| Parameter | | Min | Typ | Max | Unit |
|-----------------|--------------------------|---------------------|------|---------------------|------|
| V _{DD} | Supply Voltage | +3.0 | +3.3 | +3.6 | V |
| V _{IH} | High Level Input Voltage | 0.7 V _{DD} | - | V _{DD} | V |
| V _{IL} | Low Level Input Voltage | 0 | - | 0.3 V _{DD} | V |

7.3 DC Characteristics

(V_{DD} = 3.3V, V_{SS}=0V. T_{AMB} = 0 to 70°C)

| Parameter | | Min | Typ | Max | Unit |
|------------------|--|-----|-----|-----------------|------|
| I _{DD} | Operating Current | - | 52 | 62 | mA |
| I _{DDs} | Standby Current | - | 14 | - | mA |
| V _{OH} | Hi-level Output Voltage | 2.4 | - | V _{DD} | V |
| V _{OL} | Lo-level Output Voltage | - | - | +0.4 | V |
| I _{LI} | Input Leakage Current (No pull-up or pull-down) | -5 | - | +5 | μA |
| I _{LO} | Output Leakage Current (No pull-up or pull-down) | -5 | - | +5 | μA |
| R _L | Input Pull-up/Pull-down Resistance | | 50 | | KΩ |

1. Tested with outputs disabled (I_{OUT} = 0)
2. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.

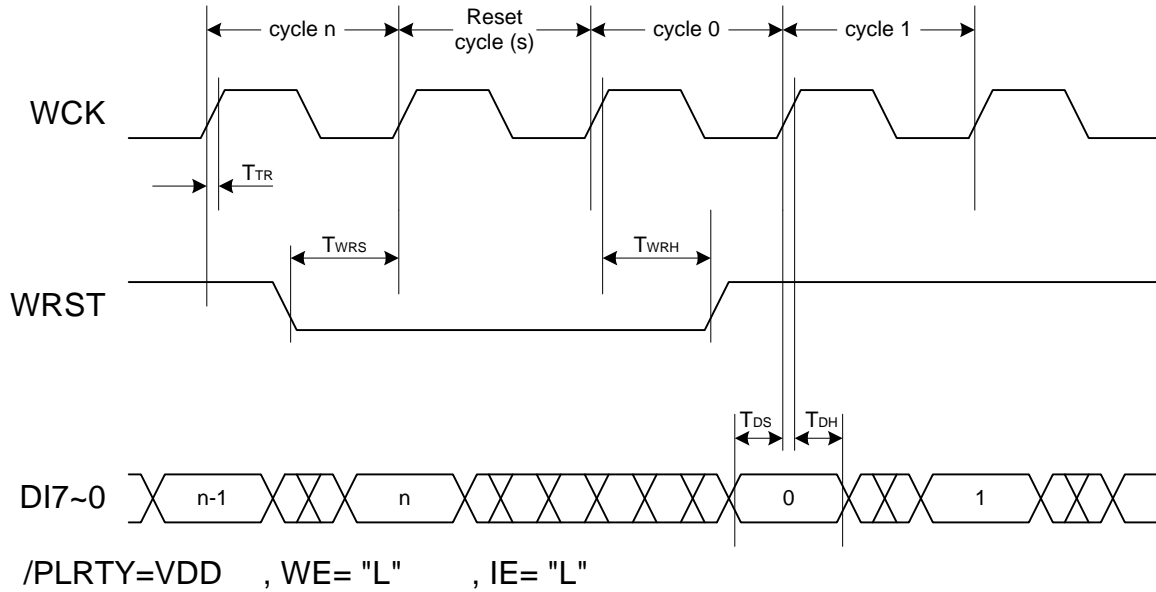
7.4 AC Characteristics

($V_{DD} = 3.3V$, $V_{SS} = 0V$, $T_{AMB} = 0$ to $70^{\circ}C$)

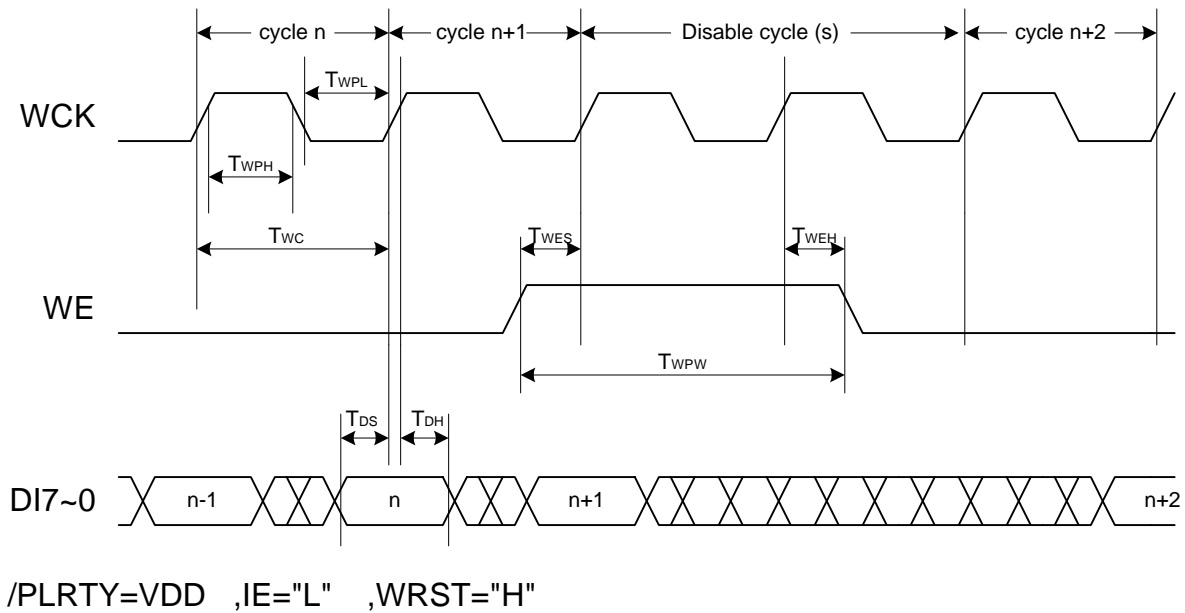
| Parameter | | 50MHz | | Unit |
|------------|--------------------------|-------|-----|------|
| | | Min | Max | |
| T_{WC} | WCK Cycle Time | 20 | - | ns |
| T_{WPH} | WCK High Pulse Width | 7 | - | ns |
| T_{WPL} | WCK Low Pulse Width | 7 | - | ns |
| T_{RC} | RCK Cycle Time | 20 | - | ns |
| T_{RPH} | RCK High Pulse Width | 7 | - | ns |
| T_{RPL} | RCK Low Pulse Width | 7 | - | ns |
| T_{AC} | Access Time | - | 15 | ns |
| T_{OH} | Output Hold Time | 4 | - | ns |
| T_{HZ} | Output High-Z Setup Time | 3 | 15 | ns |
| T_{LZ} | Output Low-Z Setup Time | 3 | 15 | ns |
| T_{WRS} | WRST Setup Time | 5 | - | ns |
| T_{WRH} | WRST Hold Time | 2 | - | ns |
| T_{RRS} | RRST Setup Time | 5 | - | ns |
| T_{RRH} | RRST Hold Time | 2 | - | ns |
| T_{DS} | Input Data Setup Time | 5 | - | ns |
| T_{DH} | Input Data Hold Time | 2 | - | ns |
| T_{WES} | WE Setup Time | 5 | - | ns |
| T_{WEH} | WE Hold Time | 2 | - | ns |
| T_{WPPW} | WE Pulse Width | 10 | - | ns |
| T_{RES} | RE Setup Time | 5 | - | ns |
| T_{REH} | RE Hold Time | 2 | - | ns |
| T_{RPPW} | RE Pulse Width | 10 | - | ns |
| T_{IES} | IE Setup Time | 5 | - | ns |
| T_{IEH} | IE Hold Time | 2 | - | ns |
| T_{IPW} | IE Pulse Width | 10 | - | ns |
| T_{OES} | OE Setup Time | 5 | - | ns |
| T_{OEH} | OE Hold Time | 2 | - | ns |
| T_{OPW} | OE Pulse Width | 10 | - | ns |
| T_{TR} | Transition Time | 2 | 20 | ns |
| C_I | Input Capacitance | - | 7 | pF |

| | | | | |
|-------|--------------------|---|---|----|
| C_o | Output Capacitance | - | 7 | pF |
|-------|--------------------|---|---|----|

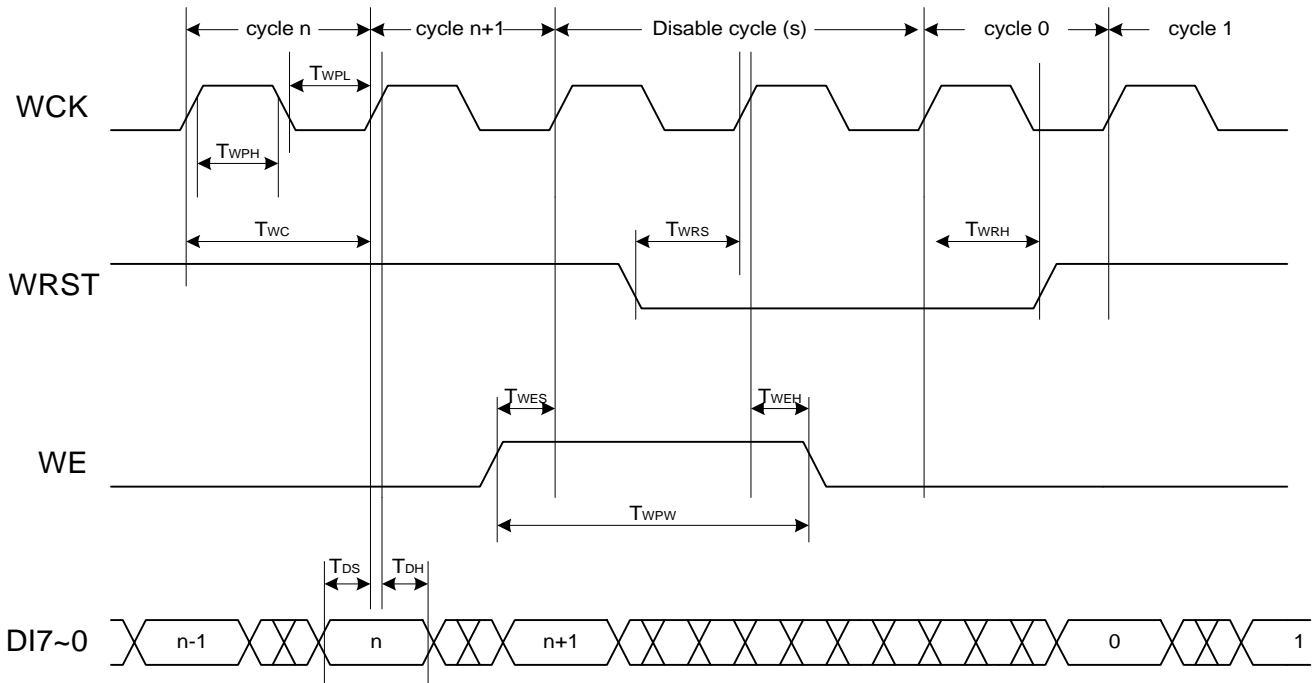
7.5 Timing Diagrams



Write Cycle Timing (Write Reset)

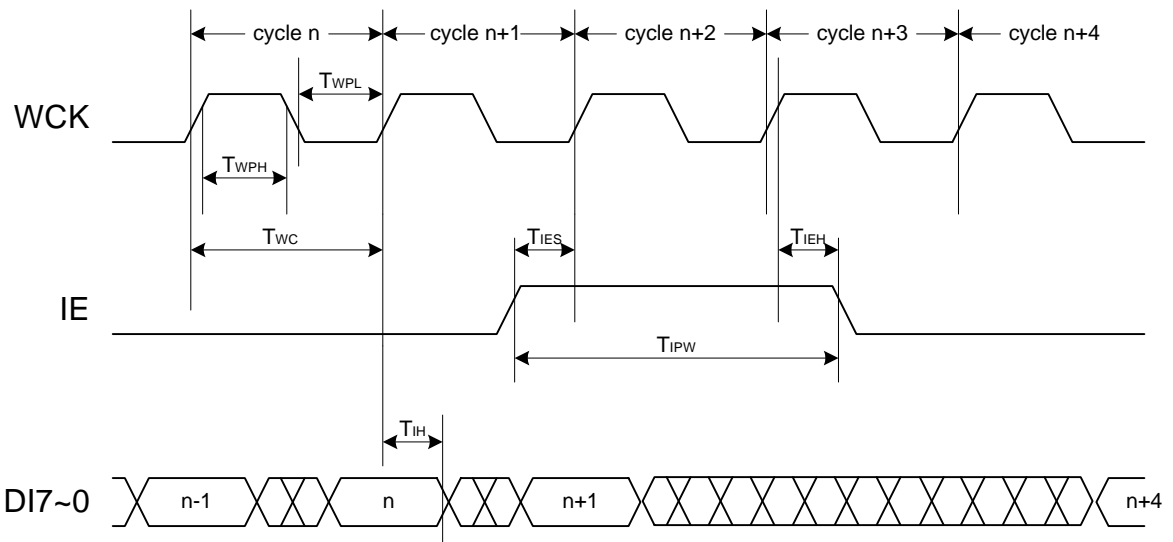


Write Cycle Timing (Write Enable)



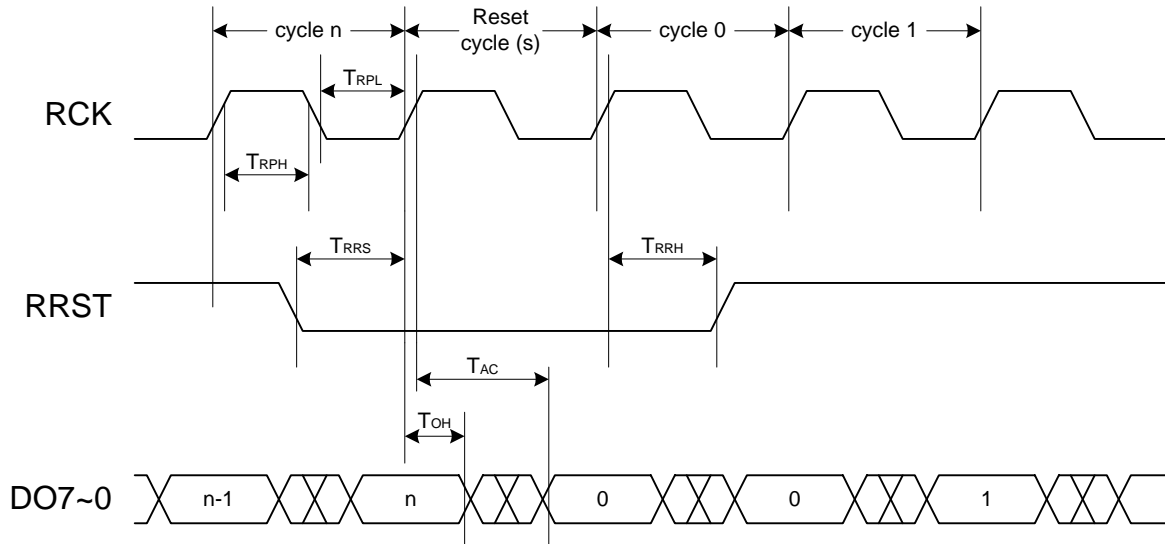
/PLRTY=VDD ,IE="L"

Write Cycle Timing (WE, WRST)



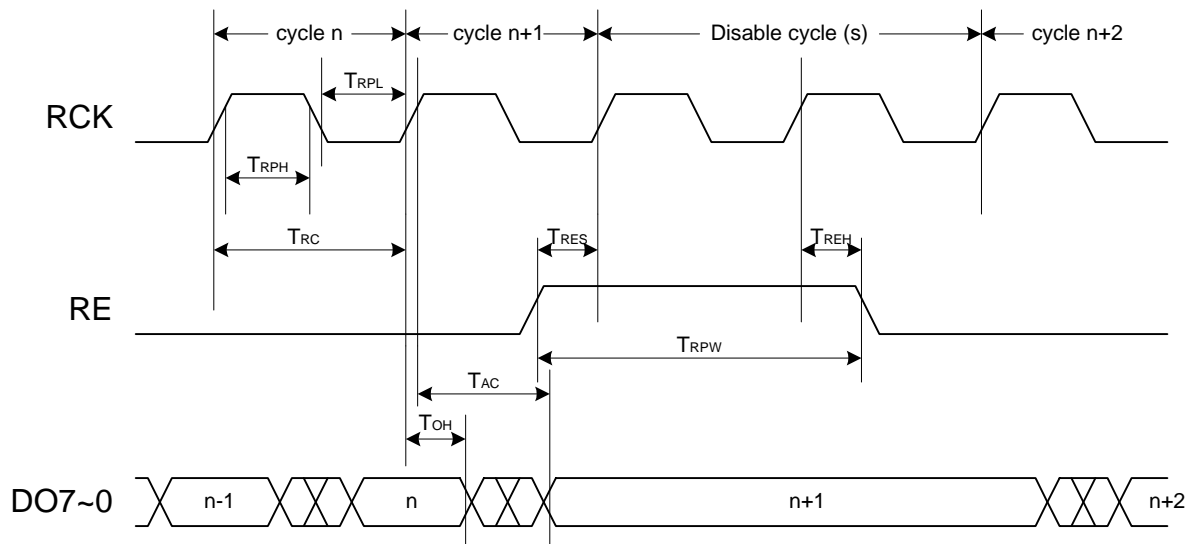
/PLRTY=VDD ,WE="L" ,WRST="H"

Write Cycle Timing (Input Enable)



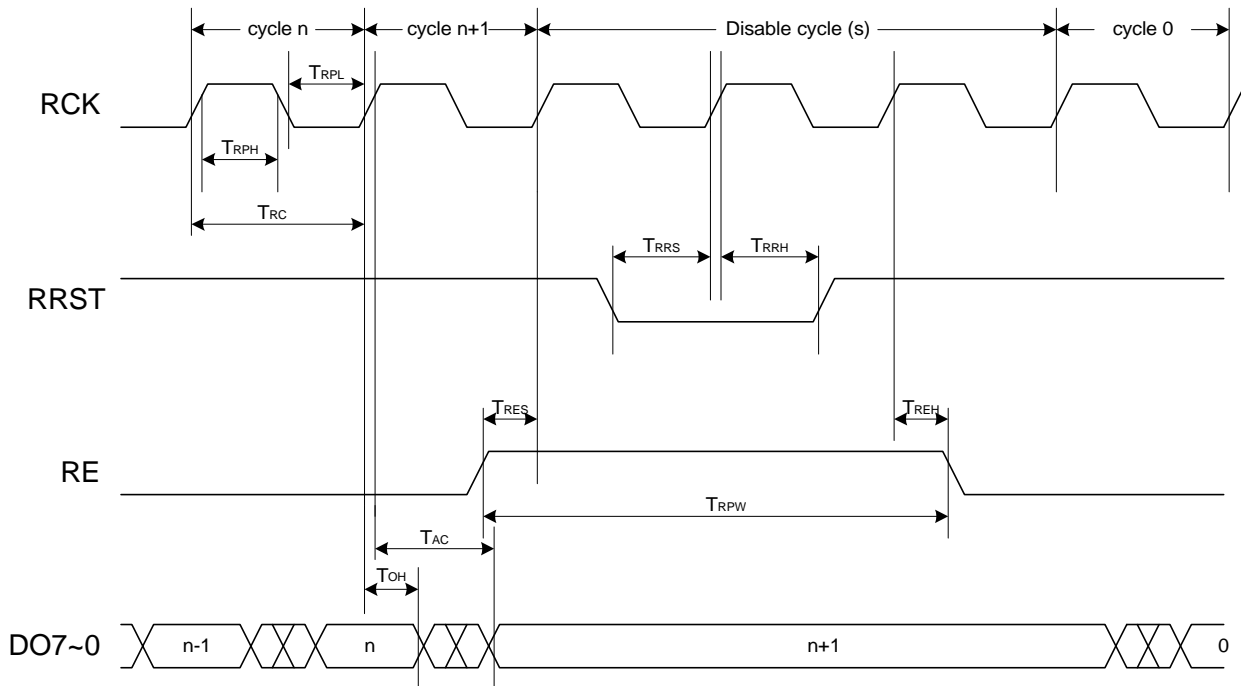
/PLRTY=VDD ,RE="L" ,OE="L"

Read Cycle Timing (Read Reset)



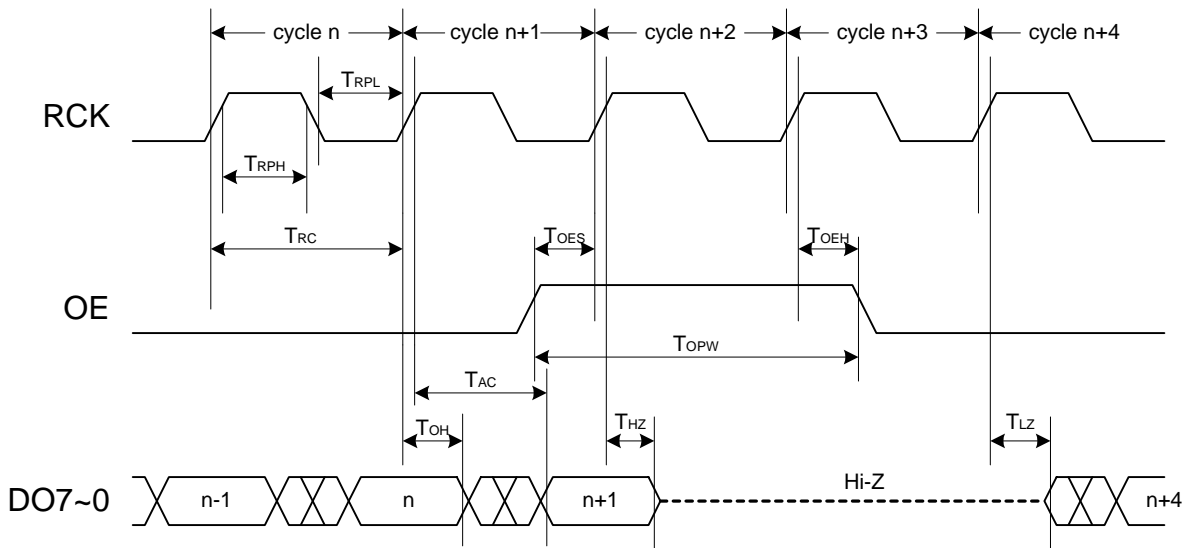
/PLRTY=VDD ,OE="L" ,RRST="H"

Read Cycle Timing (Read Enable)



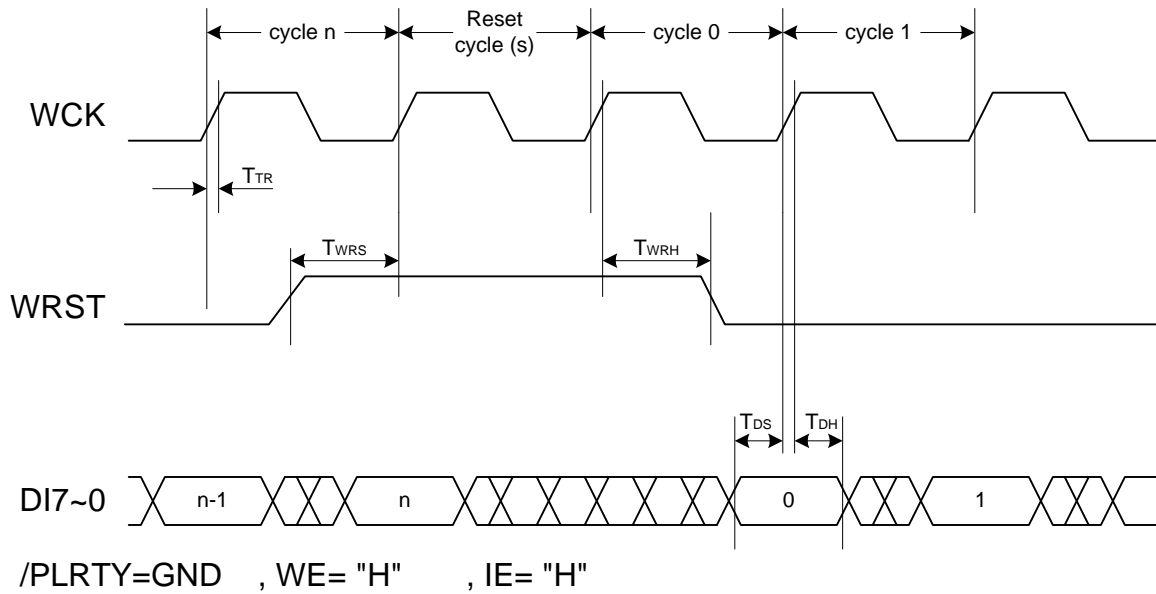
`/PLRTY=VDD ,OE="L"`

Read Cycle Timing (RE, RRST)

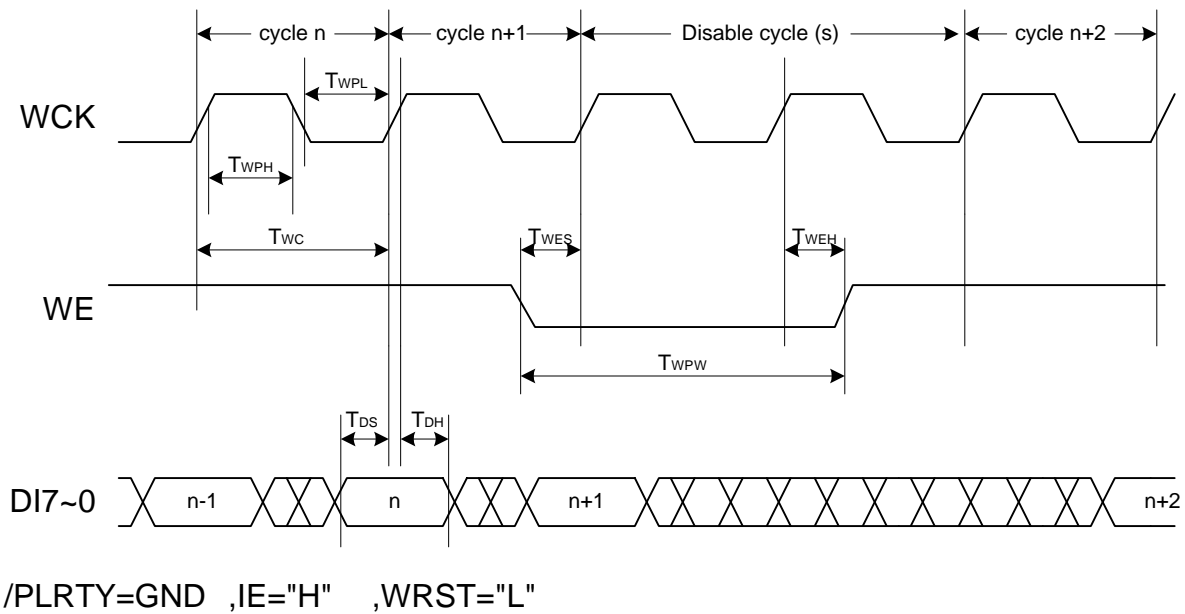


`/PLRTY=VDD ,RE="L" ,RRST="H"`

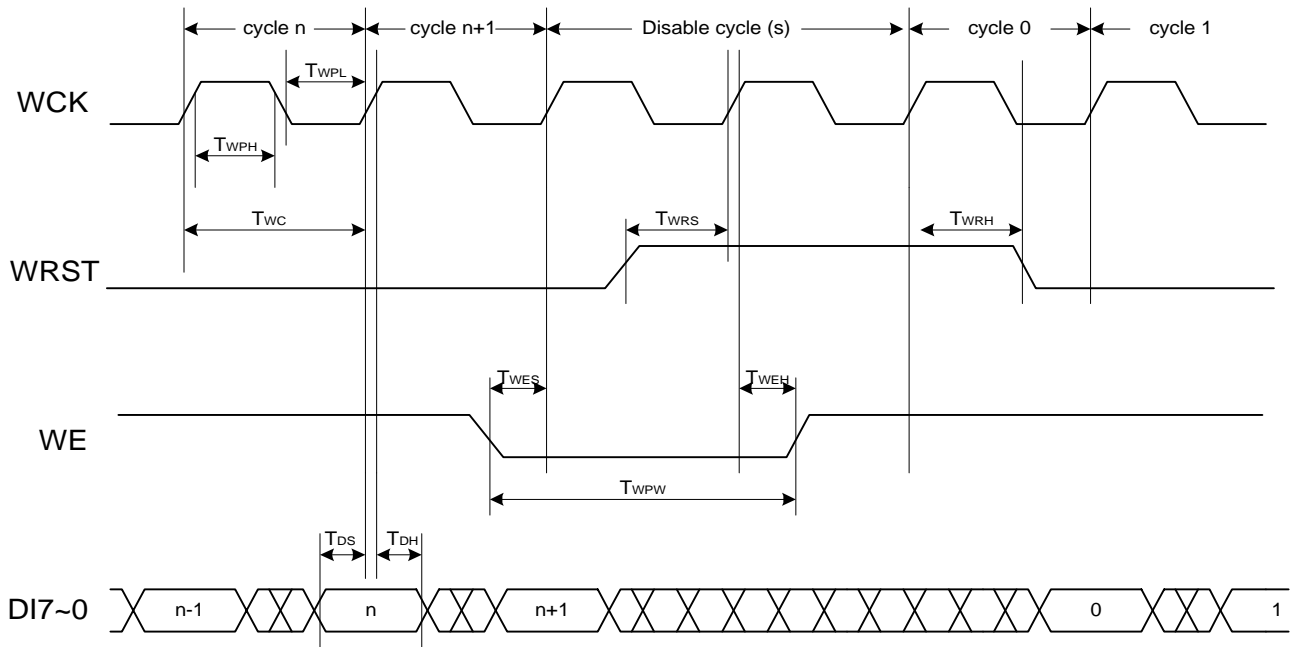
Read Cycle Timing (Output Enable)



Write Cycle Timing (Write Reset)

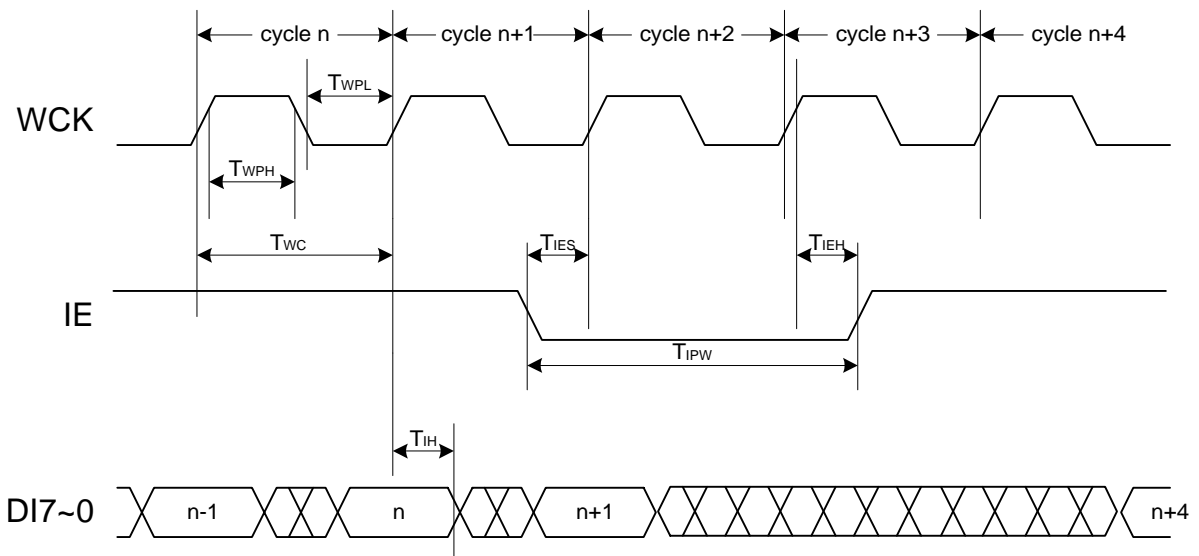


Write Cycle Timing (Write Enable)



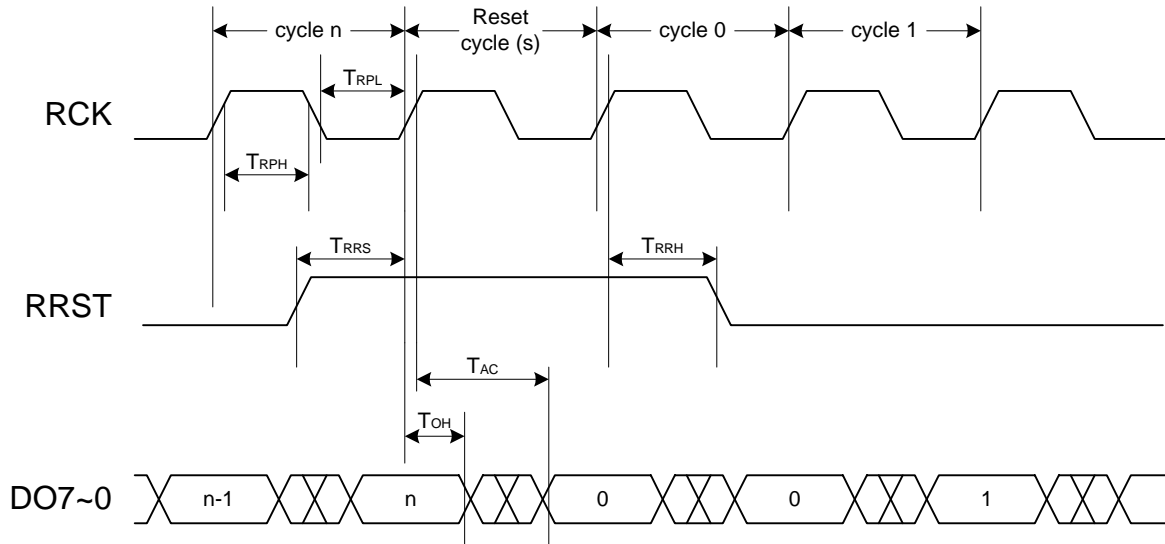
/PLRTY=GND ,IE="H"

Write Cycle Timing (WE, WRST)



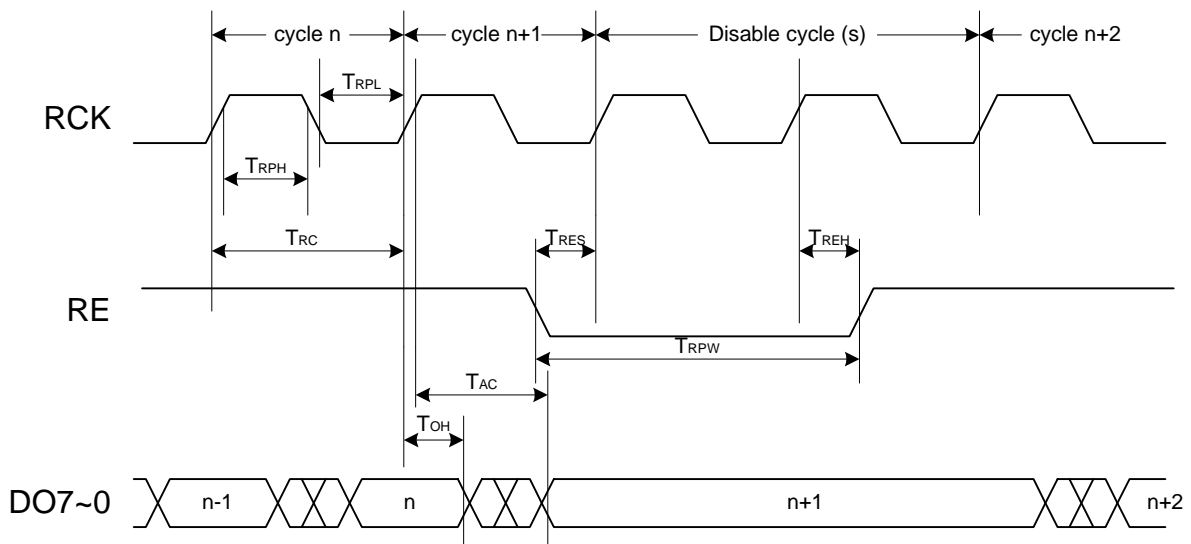
/PLRTY=GND ,WE="H" ,WRST="L"

Write Cycle Timing (Input Enable)



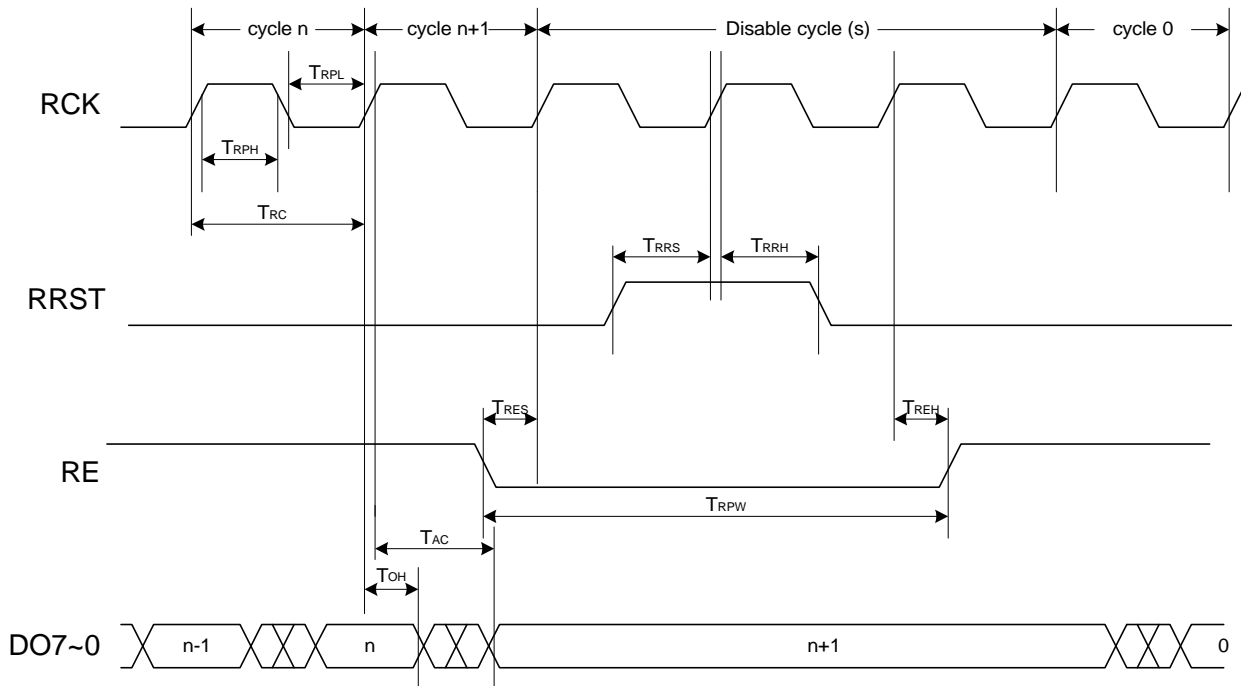
`/PLRTY=GND ,RE="H" ,OE="H"`

Read Cycle Timing (Read Reset)



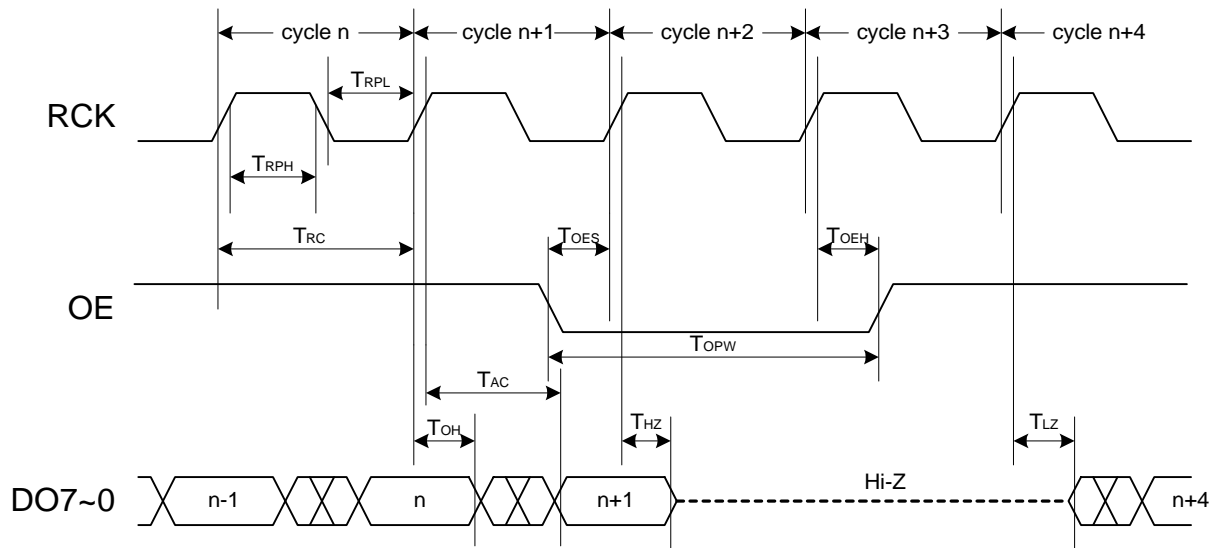
`/PLRTY=GND ,OE="H" ,RRST="L"`

Read Cycle Timing (Read Enable)



/PLRTY=GND ,OE="H"

Read Cycle Timing (RE, RRST)

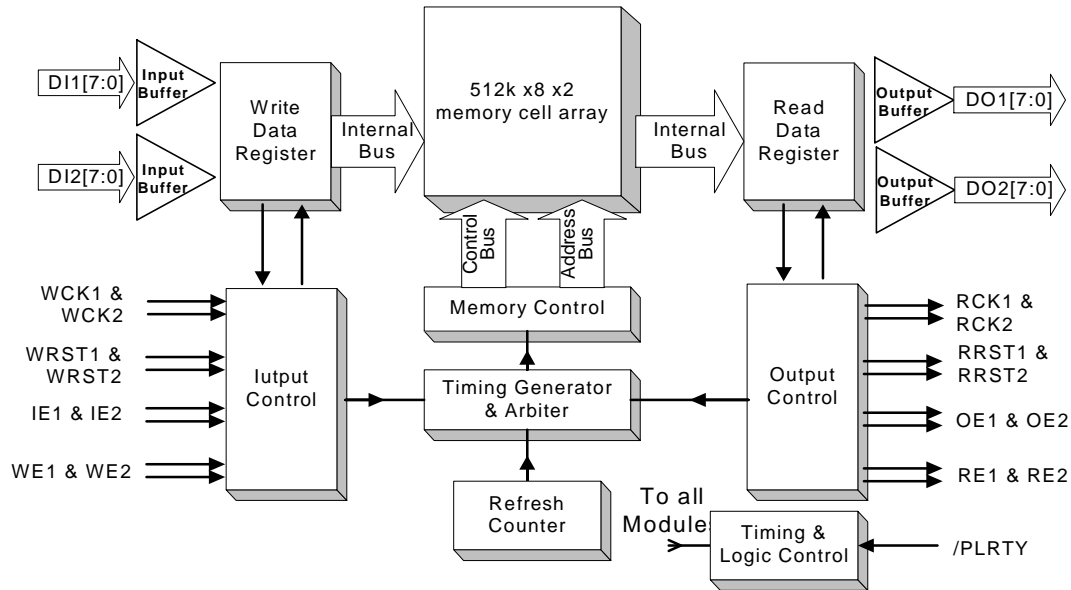


/PLRTY=GND ,RE="H" ,RRST="L"

Read Cycle Timing (Output Enable)

8.0 Block Diagram

The internal structure of each AL4V8M440x2 consists of an Input/Output buffers, Write Data Registers, Read Data Registers and main 512k x8 memory cell array and the state-of-the-art logic design that takes care of addressing and controlling the read/write data.



AL4V8M440x2 Block Diagram

9.0 Memory Operation

9.1 Power-On-Reset & Initialization

During the system power on, a 200 μ s negative pulse on the /RESET pin is required and will automatically initialize chip logic. Apply a valid reset pulse to WRST and RRST after power-on-reset to reset read/write address pointer to zero.

9.2 WRST, RRST Reset Operation

The reset signal can be given at any time regardless of the WE, RE and OE status, however, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again.

9.3 Control Signals Polarity Select

The AL4V8M440x2 provides the option for operating polarity on controlling signals. With this feature the application design can benefit by matching up the operation polarity between AL4V8M440x2 and an existing interfacing devices without additional glue logic. The operating polarity of control signals WE, RE, WRST, RRST, IE and OE are controlled by /PLRTY signal. When /PLRTY is pulled high all 8 signals will be active low. When /PLRTY is pulled low all 8 signals will be active high.

9.4 FIFO Write Operation

In the FIFO write operation, 8 bits of write data are input in synchronization with the WCK clock. The FIFO write operation is determined by WRST, WE, IE and WCK signals and the combination of these signals could produce different write result. The /PLRTY signal determines the activated polarity of these control signals. The following tables describe the WRITE functions under different operating polarities.

/PLRTY = VDD

| WRST1/ WRST2 | WE1/ WE2 | IE1/ IE2 | WCK1/ WCK2 | Function |
|-----------------|-------------|-------------|---------------|--|
| L | - | - | ↑ | Write reset. The write pointer is reset to zero. |
| H | L | L | ↑ | Normal Write operation. |
| H | L | H | ↑ | Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function) |
| H | H | - | ↑ | Write operation stopped. Write address pointer is also stopped. |

/PLRTY = GND

| WRST1/ WRST2 | WE1/ WE2 | IE1/ IE2 | WCK1/ WCK2 | Function |
|-----------------|-------------|-------------|---------------|--|
| H | - | - | ↑ | Write reset. The write pointer is reset to zero. |
| L | H | H | ↑ | Normal Write operation. |
| L | H | L | ↑ | Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function) |
| L | L | - | ↑ | Write operation stopped. Write address pointer is also stopped. |

9.5 FIFO Read Operation

In the FIFO read operation, 8 bits of read data are available in synchronization with the RCK clock. The access time is stipulated from the rising edge of the RCK clock. The FIFO read operation is determined by RRST, RE, OE and RCK signals, so the combination of these signals could produce varying read results. The /PLRTY signal could decide the activated polarity of these control signals. The following tables describe the READ functions under different operating polarities.

/PLRTY = VDD

| RRST1/ RRST2 | RE1/ RE2 | OE1/ OE2 | RCK1/ RCK2 | Function |
|-----------------|-------------|-------------|---------------|--|
| L | L | L | ↑ | Read reset. The read pointer is reset to zero. Data in the address 0 is output. |

| | | | | |
|---|---|---|---|---|
| L | L | H | ↑ | Read reset. The read pointer is reset to zero. Output is high impedance. |
| L | H | L | ↑ | Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low. |
| L | H | H | ↑ | Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low. |
| H | L | L | ↑ | Normal Read operation. |
| H | L | H | ↑ | Read address pointer increases. Output is high impedance. (Data skipping function) |
| H | H | L | ↑ | Read address pointer is stopped. Output data is held. |
| H | H | H | ↑ | Read operation stopped. Read address pointer is stopped. Output is high impedance. |

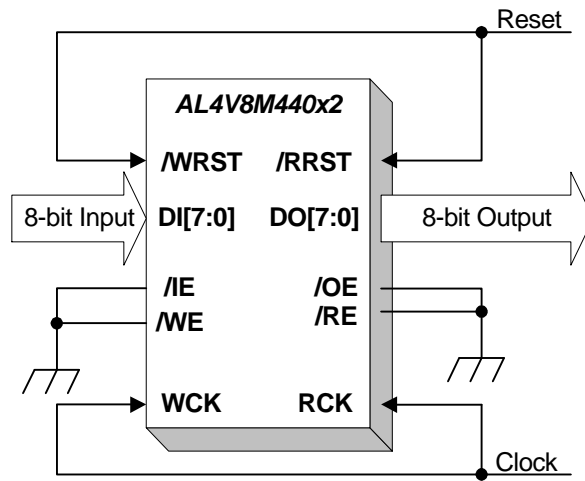
/PLRTY = GND

| RRST1/ RRST2 | RE1/ RE2 | OE1/ OE2 | RCK1/ RCK2 | Function |
|-----------------|-------------|-------------|---------------|---|
| H | H | H | ↑ | Read reset. The read pointer is reset to zero. Data in the address 0 is output. |
| H | H | L | ↑ | Read reset. The read pointer is reset to zero. Output is high impedance. |
| H | L | H | ↑ | Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low. |
| H | L | L | ↑ | Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low. |
| L | H | H | ↑ | Normal Read operation. |
| L | H | L | ↑ | Read address pointer increases. Output is high impedance. (Data skipping function) |
| L | L | H | ↑ | Read address pointer is stopped. Output data is held. |
| L | L | L | ↑ | Read operation stopped. Read address pointer is stopped. Output is high impedance. |

10.0 Application Notes

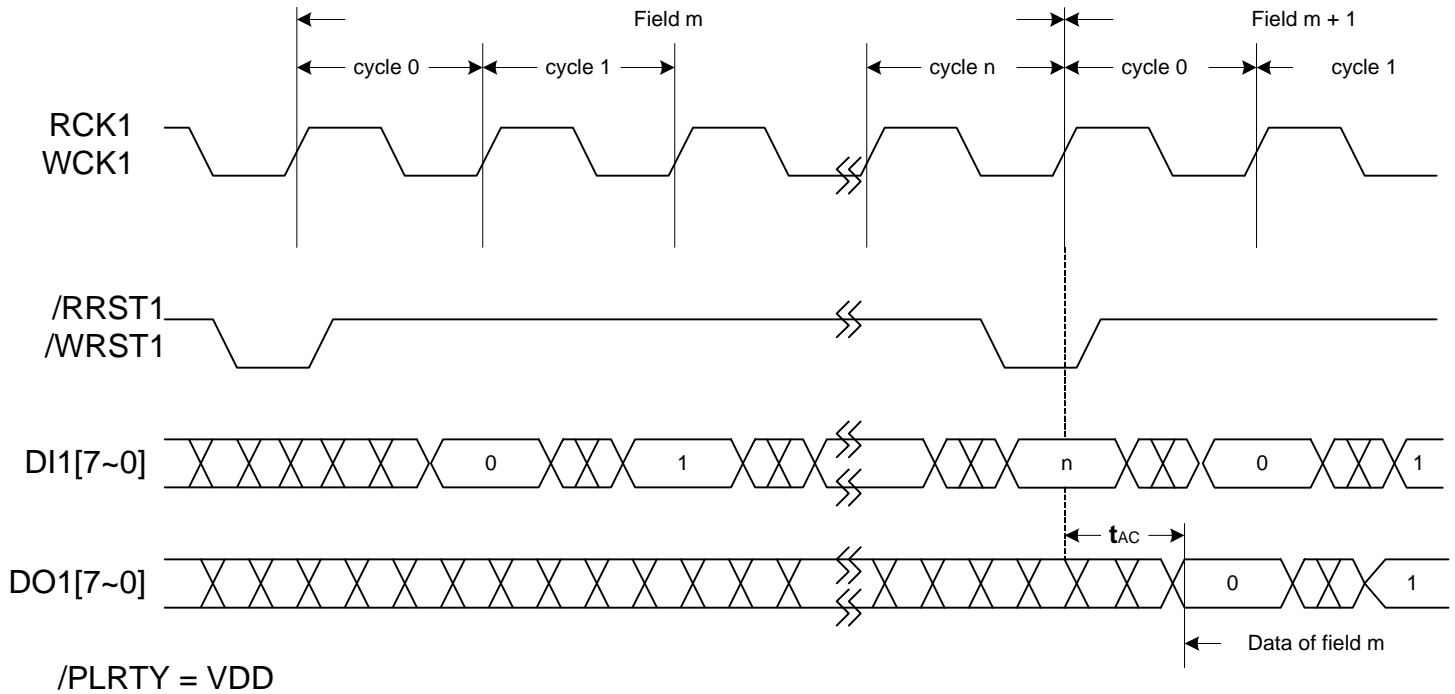
10.1 One Field Delay Line (The Old Data Read)

As the design shown in diagram by applying the reset every 1-field cycle (with the common signal for WRST and RRST) and a constant read/write operation (with all WE, RE, IE and OE are tied to active status), “1 field delay line” timing is shown in timing chart below. When the difference between the write address and the read address is 0 (the read address and the write address are the same), the old field data are read as shown in the timing chart.



Note: The connection applies to both modules

AL4V8M440x2 1 Field Delay Line Diagram

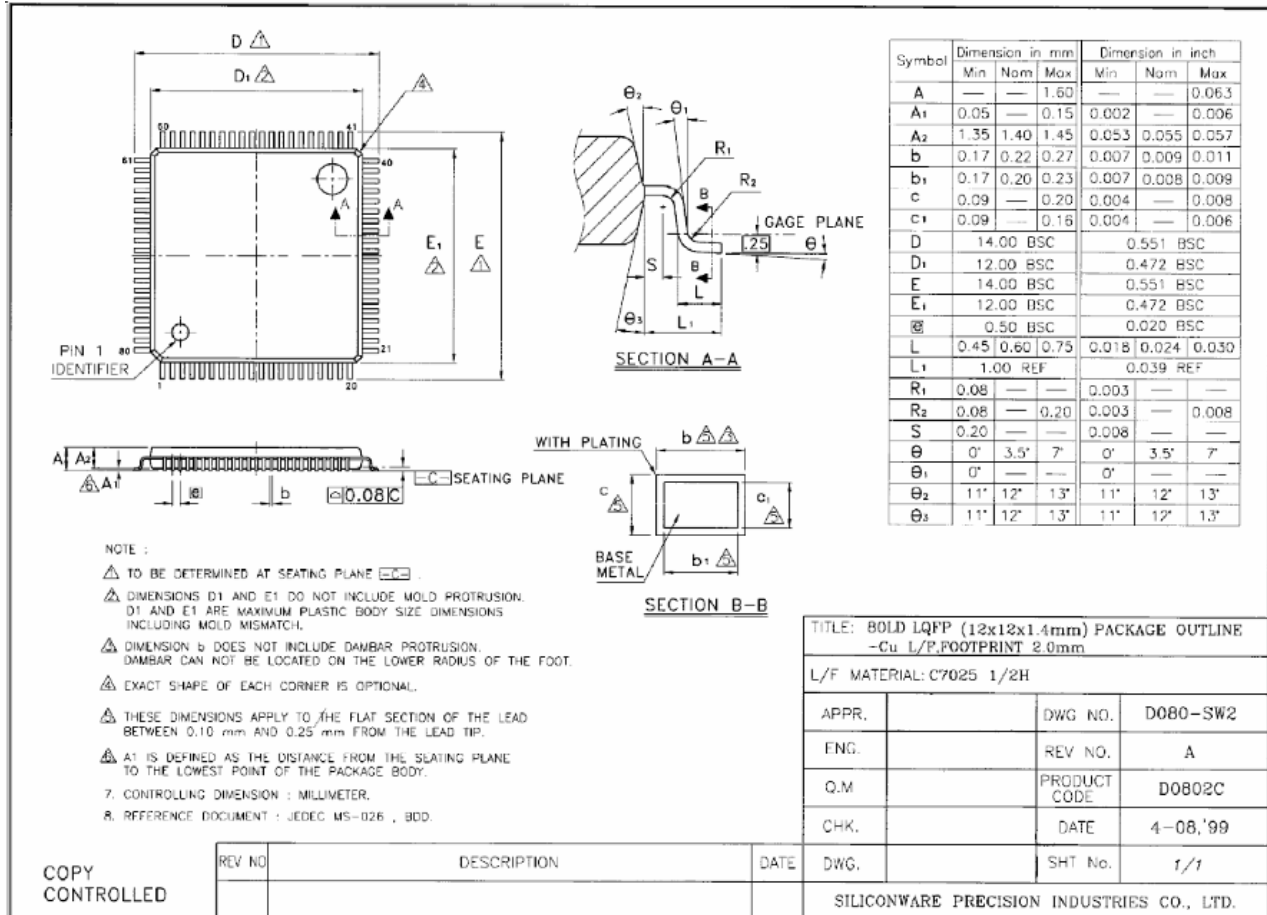


Note: The same timing also apply to module 2

AL4V8M440x2 1 Field Delay Line Timing Diagram

11.0 Mechanical Drawing – 80 PIN PLASTIC TQFP

11.1 12x12mm 80-Pin TQFP Package



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