

**Circuit Considerations for Updated
AGB64LV01 Graphical OS Chip****Introduction**

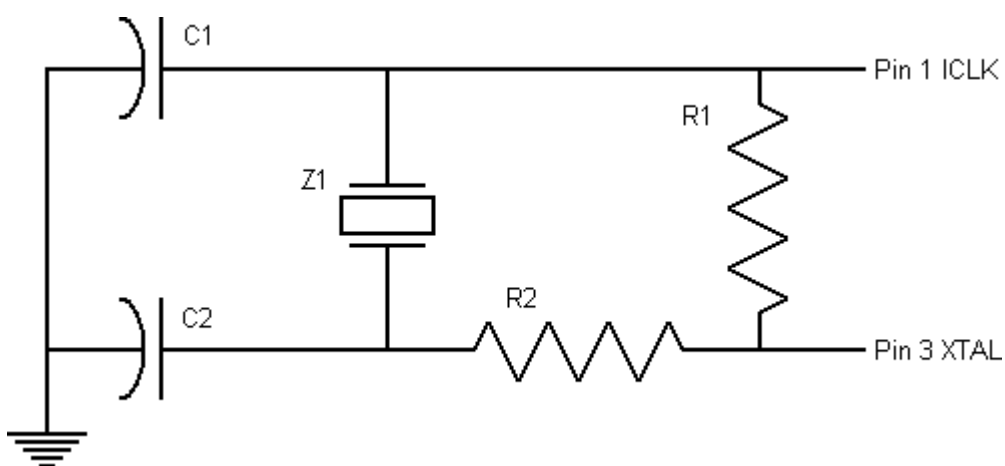
Starting September 1st, 2006, Amulet Technologies will begin shipping an updated version of its AGB64LV01 Graphical OS Chip and phasing out the previous version. By October 31st, Amulet Technologies will be shipping only the updated version of the AGB64LV01, which will maintain the same part number. The main enhancement of the updated version is an increase in programming speed while in Program Mode. Due to a new manufacturing process, the new updated version of the AGB64LV01 may potentially require one or more circuit board changes from earlier designs. If necessary, all current and future board designs should incorporate the circuit modifications immediately.

Other than a difference in internal pull-up resistance and the increase in programming speed, the chips are functionally equivalent. Like the previous version of the AGB64LV01, the new updated version is NOT 5 volt tolerant. The modifications described below will also work with all earlier versions of the AGB64LV01.

Crystal Circuit

If using a crystal instead of a clock signal to drive the AGB64LV01, the crystal circuit should be changed to match the schematic below (Figure 1). Notice the addition of resistor R2 in the crystal circuit. To filter out unwanted harmonic frequencies, use the resistor and capacitor values listed in Table 1.

Figure 1.



Recommended Crystal Component Selections

CFS1 = ¹ Amulet Pin 59
 CFS2 = ¹ Amulet Pin 60
 R1, R2 = Resistor (+/- 10%)
 C1, C2 = Capacitor (+/- 10%)

Table 1.

Z1	CFS1	CFS2	R1	R2	C1	C2
10 MHz.	High	High	1 MΩ	1.8 kΩ	18 pF	18 pF
12 MHz.	Low	High	1 MΩ	1.0 kΩ	18 pF	18 pF
16 MHz.	High	Low	1 MΩ	560 Ω	15 pF	15 pF
20 MHz.	Low	Low	1 MΩ	560 Ω	12 pF	12 pF

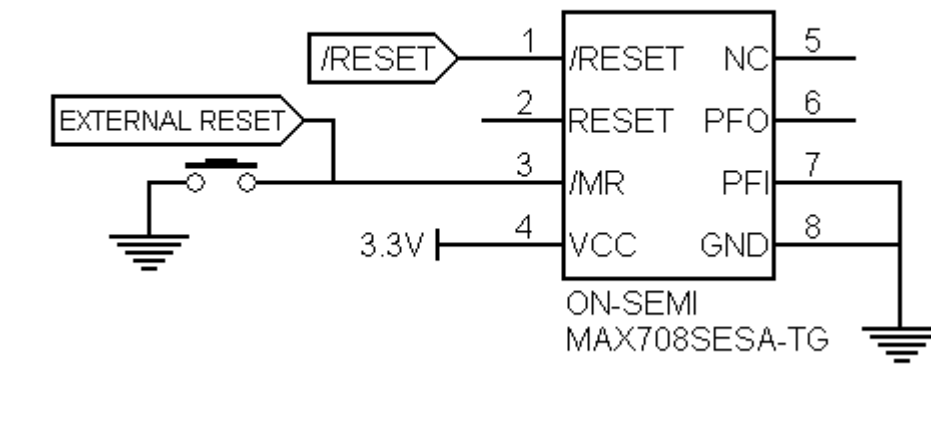
¹ By default, CFS1 and CFS2 are internally pulled high.

Reset Circuit

The AGB64LV01 uses an Atmel serial data flash that should not be accessed until after a 20ms delay once VCC is stabilized above 2.7v. If the AGB64LV01 attempts to read the serial data flash before the 20ms delay, the data may not be reliable. Due to the change in internal pull-up resistance of the new updated version, previous reset circuits might not meet the 20ms requirement. For this reason, if your processor is controlling the AGB64LV01's /RESET pin, no changes are required, assuming the /RESET pin is held low for a minimum of 20ms after power has been applied and stabilized above 2.7v.

If using an under-voltage detector, use On Semiconductor's MAX708S or an equivalent part with a delay greater than 20ms and a minimum 2.7v reset threshold level. The MAX708S has a delay of 200ms and a 2.93v reset threshold level. If using an external reset device, such as a momentary push button, connect it to /MR and ensure it is open collector.

Figure 2.





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