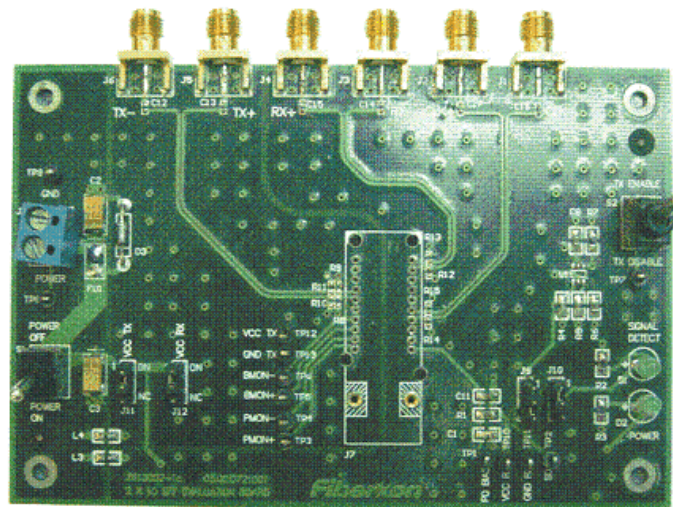


## FVB-007

### Evaluation Board For

### 2x10 Small Form Factor Transceiver

### Application Note



## Features

- ◆ **Industry standard SFF Footprint**
- ◆ **Separate powering of receiver and transmitter sections**
- ◆ **Power supply filtered separately for RX and TX side**
- ◆ **Analog diagnosis of TX and RX**
- ◆ **Clock output from CDR module**
- ◆ **TX disabled by using an assembled switch**
- ◆ **Convenient LED display for Signal Detect**
- ◆ **Internal inputs and outputs DC coupled module supported**
- ◆ **Used for either 2x5 or 2x10 pin modules**

## Overview

This evaluation board is designed for the testing and evaluation of the optical Small Form Factor (SFF) transceiver modules for data rates from 100Mbps to up to 2.5Gbps. The board accepts both the pins of a 2x5 or 2x10 SFF optical transceiver.

The board provides four 50-ohm SMA coaxial connectors (J1-J4) for the high-speed differential transmitter input signals (TX+, TX-) and receiver output signals (RX+, RX-). If SFF transceiver contains CDR module, other two 50 Ohm SMA coaxial connectors (J5, J6) are provided for the recovery clock signals (CLK+, CLK-). All high-speed inputs and outputs are transmitted by 50 Ohm transmission line on the top of the PCB.

The board has a single power supply connection (J8), of which the power side must be supplied with  $3.3V \pm 5\%$  and the other side should be connected to ground. A LED (D2) indicates the power supply. J11, J12 allow separate powering of transmitter and receiver sections.

A LED (D1) indicates the Signal Detect output of the module. As normal operation, Logic "1" outputs and the LED will light. For applications of 622Mbps and below, a converting circuit is designed to convert the PECL SD signal to TTL level. Two jumpers (J9, J10) are provided for this circuit selection. A switch is provided to assert and test the transmit disable function (S2).

A resistor (R1), supplied photocurrent, is connected to positive voltage supply and may be used to monitor received power. The current that flows into this pin is the received photocurrent. Considering the range of the received power, the value of the resistor is 2K. TP1 are provided to test the analog voltage output  $V_{pd}$ , which is proportional to the photo detector bias per the following formula:  $I_{pd} = (V_{cc} - V_{pd}) / 2K$ .

TP3 and TP4 are provided to test the analog voltage output  $V_{Pmon+}$  and  $V_{Pmon-}$ , which is proportional to the monitor photodiode current per the following formula:  $I_{MON} = (V_{Pmon+} - V_{Pmon-}) / 200$ .

TP5 and TP6 are provided to test the analog voltage output  $V_{Bmon+}$  and  $V_{Bmon-}$ , which is proportional to the laser bias current, per the following formula:  $I_{BIAS} = (V_{Bmon+} - V_{Bmon-}) / 10$ .

For SFF module with internal DC coupled outputs and inputs resistors (R8~R15) and capacitors (C12~C17) are set to meet the termination requirements of PECL I/O structure.

### Ordering Information

Internal inputs and outputs module supported	Part Number
AC Coupled	FVB-006
DC Coupled	FVB-007

### Circuit Diagram of 2x10 SFF Evaluation Board

