

## 1.32 Gbit/s Serial Link Application Kit & Twin Kit

The GigaSTaR application kit ING\_AK is a versatile and modular tool to easily adapt the 1.32 Gbit/s high-speed GigaSTaR link to any system environment or to evaluate the link under specific and predefined conditions.

The application kit supports uni- and bi-directional transmissions as well as a so called "loop-back" mode to configure a complete link with one application kit. The Twin Kit ING\_AK2 allows full duplex 1.32 Gbit/s transmissions between the two main boards.

### INTERFACES

**PC-INTERFACE (EPP):** With the supplied menu-driven software, any type of data-pattern or -sequences can be set-up to generate continuous and repeatable bursts for easy evaluation of the link and its signals.

**36 BIT PARALLEL INTERFACE:** The two external 36 bit interfaces for Transmitter and Receiver (3.3V CMOS) are FIFO buffered and allow an easy adaption of the link to any proprietary parallel interface.

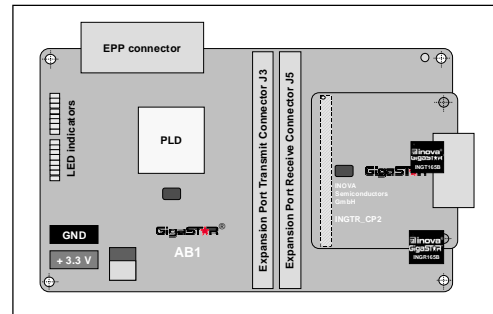
### PIGGYBACK BOARD CONCEPT

All components for the parallel-to-high-speed serialization/ de-serialization including the high-speed connector are mounted on a separate piggyback which is mounted on the main board.

The interface between the main board and the piggyback are two transparent 36 bit parallel interfaces (Tx, Rx) as described in the GigaSTaR INGT165B/INGR165B datasheet.

The piggyback board ING\_TRC shipped with the application kit contains the GigaSTaR Transmitter- and Receiver devices INGT165B & INGR165B to configure a complete link on board (loop-back).

## GigaSTAR<sup>®</sup> ING\_AK/ING\_AK2



### FEATURES

- FIFO buffered external parallel interface (512 x 36 bit)
- EPP(IEEE1284) PC interface
- Programmable operation and evaluation modes
- High-speed components on separate piggyback board
- Compact size:  
170 x 100 mm main board,  
64 x 59 mm piggyback board
- Single 3.3V DC-supply

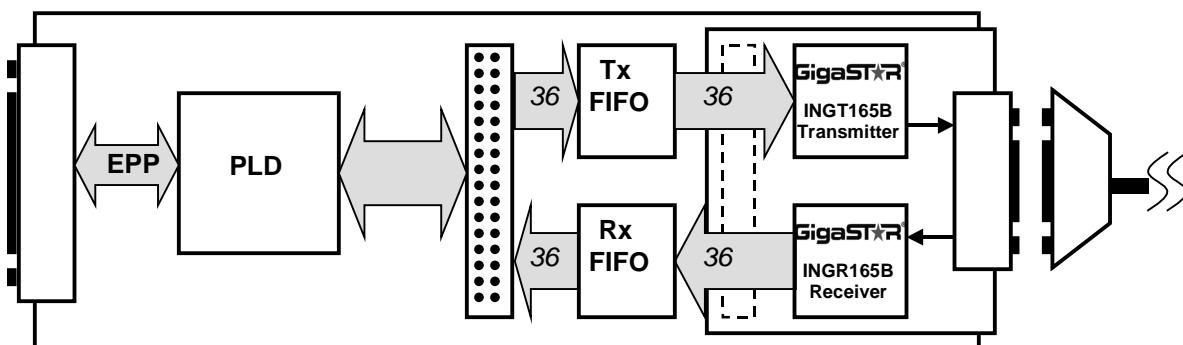
#### ING\_AK PART LIST :

- Mainboard
- Piggyback with GigaSTaR Transmitter and Receiver
- 5 m Shielded Twisted Pair Cable
- Loop-back plug, EPP PC cable
- PC Software on CD-ROM

#### ING\_AK2 PART LIST :

- 2 ING\_AK Application Kits  
plus extra 10 m STP Cable

Figure 1: Application Kit Block Diagram



## 1. GIGASTAR LINK DESCRIPTION

The GigaSTaR link is designed for reliable high-speed low-latency data transmissions. All functions for the data transfer management including the high-frequency blocks are fully integrated in the Transmitter and Receiver devices. Both devices feature a 36-bit “user-friendly” parallel interface with standard logic levels (3.3V CMOS) for easy adaptation to any application.

The link supports an effective (sustained) data rate up to 148.5 MByte/s at the parallel interface, which translates to a serial bit stream of max. 1.188 Gbit/s (payload data rate). With 4 additional bits for link-synchronization, DC-balancing and parity check the maximum bit rate at the serial I/Os is 1.32Gbit/s, for an overall link efficiency of 90 percent. With only 40 ns propagation delay time each for the Transmitter and Receiver, the typical overall latency for a GigaSTaR link is:

$$\text{latency [ns]} = 2 * 40 \text{ ns} + 4\text{ns/m} * \text{cable-length [m]}$$

For example, the latency is about 160 ns for a 20 meter connection with Shielded-Twisted-Pair (STP) copper cable.

### 1.1 CLOCK SYSTEM

The serial bit clock frequency of 1320 MHz is generated by internal PLLs. The Transmitter and Receiver are each clocked by an external 66 MHz reference clock.

A continuous phase alignment in the Receiver ensures that the receive clock is synchronous to the transmit clock.

### 1.2 PARALLEL DATA FORMAT

Both the GigaSTaR Transmitter and Receiver feature a synchronous 36 bit parallel interface. The maximum frequency at this interface is 33 MHz, equivalent to a period of 30.3 ns for the WRCLK/ RDCLK signals.

Additional parity I/Os allow the transfer of an optional external parity bit synchronous with the parallel data. If an external parity bit is provided, the Transmitter validates the signal before the start of the transmission. If no external parity bit is available, the Transmitter generates this signal automatically. Parity error flags are provided at both the Transmitter and Receiver devices.

### 1.3 SERIAL DATA FORMAT

The serial data stream is DC-balanced to support capacitive (AC) coupling for full DC isolation of the link. This is performed by proprietary coding in the Transmitter device.

### 1.4 LINK MEDIA (COPPER OR FIBER)

The GigaSTaR Transmitter and Receiver are each equipped with a robust high-speed interface which can be directly connected to impedance-controlled cables (STP or coax), transmission lines or fiber optic modules.

Initial evaluations with 50 Ohm (100 Ohm differential) Shielded-Twisted-Pair (STP) cables already have proven reliable transmissions at distances of up to 30 meters (Reference-product: GGSC1608-05/-10/-15/-20/-25/-30, W.L. Gore & Associates).

With conventional 850 nm fiber optic modules (AC in/out, 3.3V PECL) and multimode fiber distances above 300 meters (max. 500 meters) have been achieved.

## 1.5 TECHNICAL DETAILS

For more technical details, please refer to the GigaSTaR ING165B\_DS and the ING\_TRC\_DS datasheets. For a description of the Application kit operating modes, please refer to the GigaSTaR Application Kit User Manual ING\_AK\_UM. Please check our website for the latest revisions of these documents at :

<http://www.inova-semiconductors.com> .

## 2. CONNECTOR DEFINITIONS

### 2.1 TRANSMITTER (TX) FIFO RIBBON CABLE CONNECTOR J3

Pin	Signal	Dir.	Description
1	GND	OUT	Ground
2-37	TXFD0 - 35	IN	Transmit Fifo Data Input. Data is posted into the Fifo on rising edge of TF_LDCK
38	TX_PARITY	IN	GigaSTaR Transmitter Parity Input. Don't care when PARGEN=1
39	GND	OUT	Ground
40	CLK33	OUT	Application baseboard clock; 33 MHz
41	VCC	OUT	+3.3 V
42	EXPANSION	IN	Needs to be connected to VCC to force MACH Output Signal into tri-state
43	GND	OUT	Ground
44	RDCLK	OUT	GigaSTaR Transmitter Read Clock. Clocks data out of the Fifo on rising edge
45	GND	OUT	Ground
46	TX_PERR#	OUT	GigaSTaR Transmitter Parity Error
47	TX_LOCK	OUT	GigaSTaR Transmitter PLL Lock Indication. 1:Pll locked; 0:Pll unlocked
48	FLAGI	IN	GigaSTaR Transmitter FLAGI Signal
49	VALID	IN	Signals to GigaSTaR that valid data is available at Fifo output. Starts transmission
50	TF_FULL	OUT	Transmit Fifo Full
51	TF_AF	OUT	Transmit Fifo Almost Full. Low: 64 < Words posted in FIFO < 512-64
52	TF_EMPTY	OUT	Transmit Fifo Empty
53	TF_RST	IN	Transmit Fifo Reset
54	TF_LDCK	IN	Transmit Fifo Load Clock
55	NC		Not connected
56	TX_RESET#	IN	GigaSTaR Transmitter Reset
57	RESERVED	OUT	Reserved
58	PARGEN	IN	GigaSTaR Transmitter Parity Generation Mode: 1: generate parity
59	RESERVED	IN	Reserved for optional function, has to be set to '0'
60	VCC	OUT	+3.3 V
61	SPARE1		
62	SPARE2		
63	RESET#	OUT	Application Baseboard Reset
64	GND	OUT	Ground

Table 1: Transmitter (Tx) Fifo Ribbon Cable Connector Definition

## 2.2 RECEIVER (RX) FIFO RIBBON CABLE CONNECTOR J5

Pin	Signal	Dir.	Description
1	GND	OUT	Ground
2-37	RXFQ0 - 35	OUT	Receive Fifo Data Output. Data is read out of the Fifo on rising edge of TF_UNCK
38	RX_PARITY	OUT	GigaSTaR Receiver Parity Output.
39	GND	OUT	Ground
40	CLK33	OUT	Application baseboard clock; 33 MHz
41	VCC	OUT	+3.3 V
42	EXPANSION	IN	Needs to be connected to VCC to force MACH Output Signal into tri-state.
43	GND	OUT	Ground
44	WRCLK	OUT	GigaSTaR Receiver Write Clock. Signals valid data on receiver parallel interface
45	GND	OUT	Ground
46	RX_PERR#	OUT	GigaSTaR Receiver Parity Error
47	RX_LOCK	OUT	GigaSTaR Receiver PLL Lock Indication. 1: Pll locked; 0:Pll unlocked
48	FLAGO	OUT	GigaSTaR Receiver FLAGO Signal
49	RX_LSYNC#	OUT	GigaSTaR Receiver Frame Synchronization Status. 0: sync; 1: not sync
50	RF_FULL	OUT	Receive Fifo Full
51	RF_AF	OUT	Receive Fifo Almost Full. Low: 64 < Words posted in FIFO < 512-64
52	RF_EMPTY	OUT	Receive Fifo Empty
53	RF_RST	IN	Receive Fifo Reset
54	RF_UNCK	IN	Receive Fifo Unload Clock
55	RF_LDCK	IN	Receive Fifo Load Clock. Should be triggered by WRCLK
56	RX_RESET#	IN	GigaSTaR Receiver Reset
57	EQSEL	IN	GigaSTaR Receiver Equalizer Select: 1: Equalizer is selected
58	VCC	OUT	+3.3V
59	SPARE1		
60	VCC	OUT	+3.3V
61	SPARE2		
62	SPARE3		
63	RESET#	OUT	Application Baseboard Reset
64	GND	OUT	Ground

Table 2: Receiver (Rx) Fifo Ribbon Cable Connector Definition

## 2.3 PIGGYBACK BOARD 140 PIN AMP CONNECTOR J4

Pin	Signal	Pin	Signal	Pin	Signal
4	TXPD0	82	RXPD0	2	GND
6	TXPD1	84	RXPD1	11	GND
8	TXPD2	86	RXPD2	22	GND
10	TXPD3	88	RXPD3	31	GND
14	TXPD4	92	RXPD4	42	GND
16	TXPD5	94	RXPD5	51	GND
18	TXPD6	96	RXPD6	61	GND
20	TXPD7	98	RXPD7	65	GND
13	TXPD8	93	RXPD8	69	GND
15	TXPD9	95	RXPD9	73	GND
17	TXPD10	97	RXPD10	79	GND
25	TXPD11	103	RXPD11	90	GND
19	TXPD12	101	RXPD12	99	GND
24	TXPD13	102	RXPD13	110	GND
26	TXPD14	104	RXPD14	119	GND
28	TXPD15	106	RXPD15	130	GND
30	TXPD16	108	RXPD16	139	GND
27	TXPD17	105	RXPD17	1	VCC
29	TXPD18	107	RXPD18	12	VCC
34	TXPD19	112	RXPD19	21	VCC
33	TXPD20	111	RXPD20	32	VCC
36	TXPD21	114	RXPD21	41	VCC
37	TXPD22	115	RXPD22	52	VCC
38	TXPD23	116	RXPD23	62	VCC
35	TXPD24	113	RXPD24	80	VCC
39	TXPD25	117	RXPD25	89	VCC
40	TXPD26	118	RXPD26	100	VCC
44	TXPD27	122	RXPD27	109	VCC
45	TXPD28	123	RXPD28	120	VCC
54	TXPD29	132	RXPD29	129	VCC
48	TXPD30	126	RXPD30	140	VCC
53	TXPD31	131	RXPD31	23	Reserved, set to GND (*)
47	TXPD32	125	RXPD32	63	Reserved, set to VCC (*)
56	TXPD33	134	RXPD33	67	Reserved, do not connect (*)
49	TXPD34	127	RXPD34	71	Reserved, do not connect (*)
55	TXPD35	133	RXPD35	57, 59, 60	Not connected
7	TX_LOCK	87	RX_LOCK	64, 66, 68	Not connected
9	TX_PARITY	91	RX_PARITY	70, 72, 74	Not connected
58	TX_PERR#	136	RX_PERR#	75, 76, 77	Not connected
3	TX_RESET#	81	RX_RESET#	78, 124	Not connected
5	RDCLK	83	WRCLK	135, 137	Not connected
43	FLAGI	121	FLAGO	138	Not connected
46	PARGEN	85	EQSEL		Not connected
50	VALID	128	LSYNC#		(*) : These pins are reserved for optional functions

Table 3: Piggyback board 140 pin Connector J4 (AMP Free Height Receptable 177983-6) Pin Definition

### 3. APPLICATION KIT SPECIFICATION

#### 3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect board reliability. Functional operation of the board at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V <sub>CC</sub>	-0.5	+4.2	V	
Input Voltage	V <sub>IN</sub>	-0.5	V <sub>CC</sub> +0.5	V	
I/O Current (DC or transient any pin)	I <sub>D</sub>	-20	+20	mA	
Ambient Temperature (under bias)	T <sub>B</sub>	0	+70	°C	
Storage Temperature	T <sub>stg</sub>	-40	+100	°C	
Static Discharge Voltage (all connector pins except DB9 pins)	V <sub>SDCON</sub>		±1000	V	Human Body Model
Static Discharge Voltage (DB9 connector pins)	V <sub>SDDB9</sub>		±800	V	Human Body Model

Table 4: Absolute Maximum Ratings

#### 3.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V <sub>CC</sub>	+3.15	+3.45	V	
Input Voltage	V <sub>IN</sub>	0	V <sub>CC</sub>	V	V <sub>CC</sub> = 3.3V ± 0.15V
Ambient Temperature	T <sub>a</sub>	0	+35	°C	

Table 5: Recommended Operating Conditions

#### 3.3 ELECTRICAL SPECIFICATION

##### 3.3.1 AC – Characteristics (under recommended operating conditions)

Parameter	Min.	Typ.	Max.	Units
Input capacitance, any Expansion port pin		10		pF
Serial Transmission Data Rate		1.32		Gbit/s
Serial Payload Data Rate		1.188		Gbit/s
Parallel Interface Data Rate		148.5		MByte/s
Serial Bit Width		757.6		ps
CMOS Output Rise / Fall Time (C <sub>L</sub> at Exp. port pin : 10 pF)		5	10	ns

Table 6: AC - Characteristics

##### 3.3.2 DC – Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Expansion Port Input High Voltage	V <sub>IH</sub>		2.6			V
Expansion Port Input Low Voltage	V <sub>IL</sub>				0.8	V
Expansion Port Input Leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		1	10	µA
High-level Expansion Port Output current	I <sub>OH</sub>	V <sub>OH</sub> = 2.4 V	8	12		mA
Low-level Expansion Port Output current	I <sub>OL</sub>	V <sub>OH</sub> = 0.4 V	8	12		mA
Supply Current	I <sub>CC</sub>	Max. transmission rate		850	1000	mA
Power Dissipation	P <sub>D</sub>	Max. transmission rate		2,8	3,45	W

Table 7: DC - Characteristics

### 3.3.3 Expansion Port Transmit Path Timing (J3)

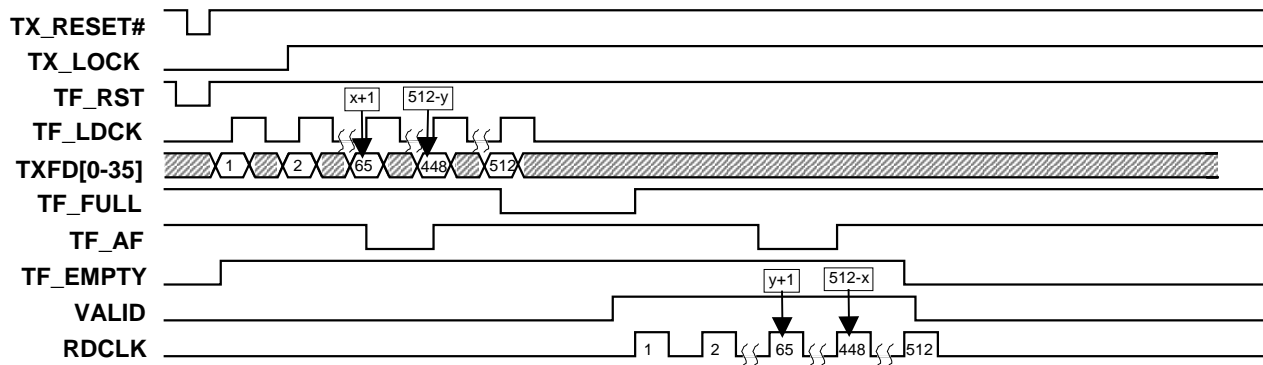


Figure 2: Timing of Direct Transmit Fifo Access through Expansion Port

The TF\_AF flag has two programmable limits : the almost-empty offset value (x) and the almost-full offset value (y). The TF\_AF flag is high when the FIFO contains X or less words respectively contains 512 minus y or more words. In figure 2, this is shown for x = y = 64 . The values x and y have to be programmed after each FIFO Reset and before the first word is written to memory.

After a FIFO reset, at the first low-high transition of TF\_LDCK, the binary value on D0-D7 is stored as the almost-empty offset value (x). At the second low-high transition of TF\_LDCK, the binary value on D0-D7 is stored as the almost-full offset value (y).

Note : When using the expansion ports for data transmission, the internal parity generation has to be used (set pin 58 of expansion port J3 to '1') .

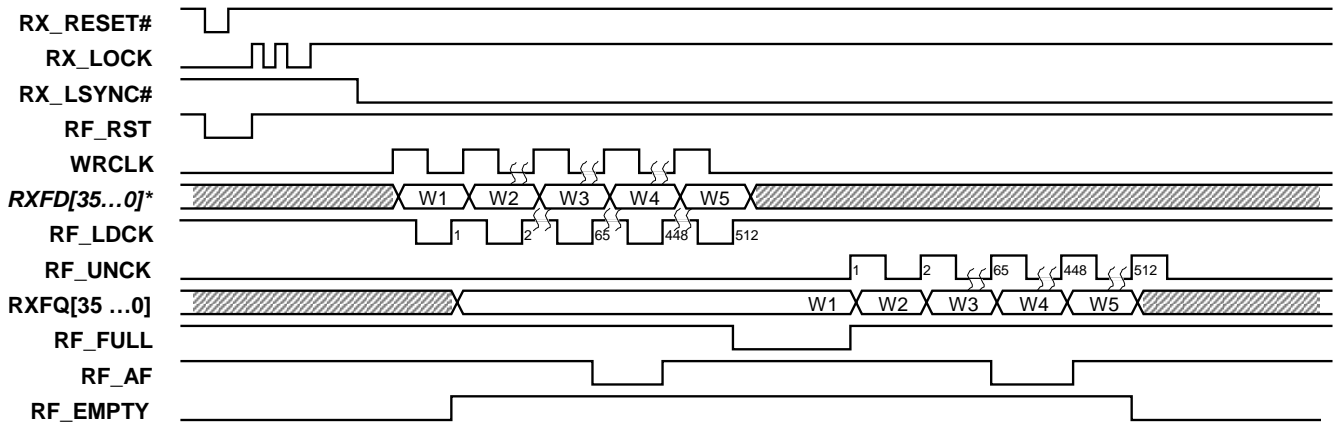
Parameter	Signal	Min.	Max.	Unit
$t_{pw}$ Pulse width	TXFD[0-35] low or high	8		ns
	TF_LDCK low or high	8		
	TF_RST low	10		
	TX_RESET# low	10		
	VALID high	8		
$t_{su}$ Setup time	TXFD0-35 before TF_LDCK $\uparrow$	5		ns
$t_{hd}$ Hold time	TXFD0-35 after TF_LDCK $\uparrow$	0		ns

Table 8: AC Operating Conditions Transmit Fifo

Parameter	From In	To Out	Min.	Max.	Unit
$f_{max}$	TF_LDCK			40	MHz
$t_{pd}$	TF_LDCK $\uparrow$	TF_AF	7	20	ns
		TF_EMPTY	6	17	
		TF_FULL	6	17	
	TF_RST low	TF_AF	2	12	ns
		TF_EMPTY	4	18	
		TF_FULL	4	20	
		VALID $\uparrow$	RDCLK $\uparrow$	11	15

Table 9: Switching Characteristics Transmit Fifo

### 3.3.4 Expansion Port Receive Path Timing



\* RXFD[35...0]: Received data input to the FIFO.  
These data are not provided at the ribbon cable connector.

Figure 3: Timing of direct Receive Fifo Access through Expansion Port

Parameter	Signal	Min.	Max.	Unit
t <sub>pw</sub> Pulse width	RF_UNCK low or high	8		ns
	RF_LDCK low or high	8		
	RF_RST low	10		
	RX_RESET# low	10		
t <sub>su</sub> Setup time	RXFD[35...0] before RF_LDCK	5		ns
t <sub>hd</sub> Hold time	RXFD[35...0] after RF_LDCK	0		ns

Table 10: AC Operating Conditions Receive Fifo

Parameter	From In	To Out	Min.	Max.	Unit	
f <sub>max</sub>	RF_UNCK, RF_LDCK			40	MHz	
t <sub>pd</sub>	WRCLK ↑	RXFD[35...0]	-3	+3	ns	
		RF_LDCK ↑	RXFQ[35...0]	9		22
			RF_AF	7		20
			RF_EMPTY	6		17
	RF_FULL		6	17		
	RF_UNCK ↑	RXFQ[35...0]	6	18		
		RF_AF	7	20		
		RF_EMPTY	6	17		
		RF_FULL	6	17		
	RF_RST low	RF_AF	2	12		
		RF_EMPTY	4	18		
		RF_FULL	4	20		

Table 11: Switching Characteristics Receive Fifo

## 4. BOARD DIMENSIONS

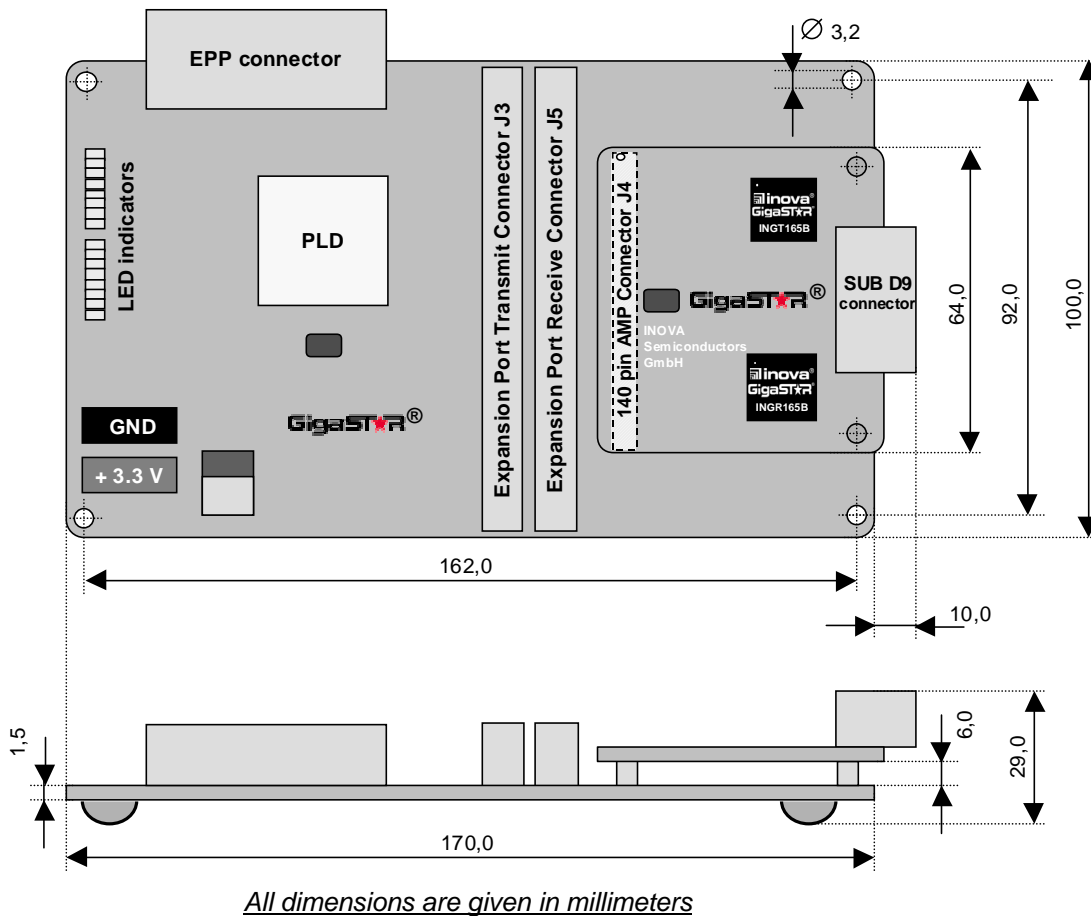


Figure 4: Top and side view of the Main Board (with mounted Piggyback Board) with mechanical outlines

## 5. HANDLING PRECAUTIONS

Handling precautions are:

1. The board does not contain protection against reverse supply polarity, please check polarity carefully before connecting.
2. The maximum ratings may not be exceeded at any time.
3. Precautions have to be taken against exposure of device terminals to electrostatic discharge stress.
4. This board is designed for the purpose of electrical evaluation in an engineering environment and has not been EME-shielded. It must not be used in an environment where its electromagnetic emissions could impact the functions of other systems or devices.
5. The voltage supply should be properly filtered to avoid a deterioration of the bit error rate due to supply voltage spikes.
6. Mounting and dismounting of the piggyback board has to be performed with care. These mounting/dismounting cycles should be limited in order to avoid AMP 140 pin connector wearout.

## 6. ORDERING CODE AND PRODUCTION STATUS INFORMATION

Ordering Code	Delivery	Production Status
ING_AK	Application Kit (part list see page 1)	Released to production
ING_AK2	Application Twin Kit (part list see page 1)	Released to production

Table 12: Product Availability

### Inova Semiconductors GmbH

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D-81675 Munich, Germany  
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