

GigaSTAR[®]

Application Kit User Manual

Revision 1.6

March 2001

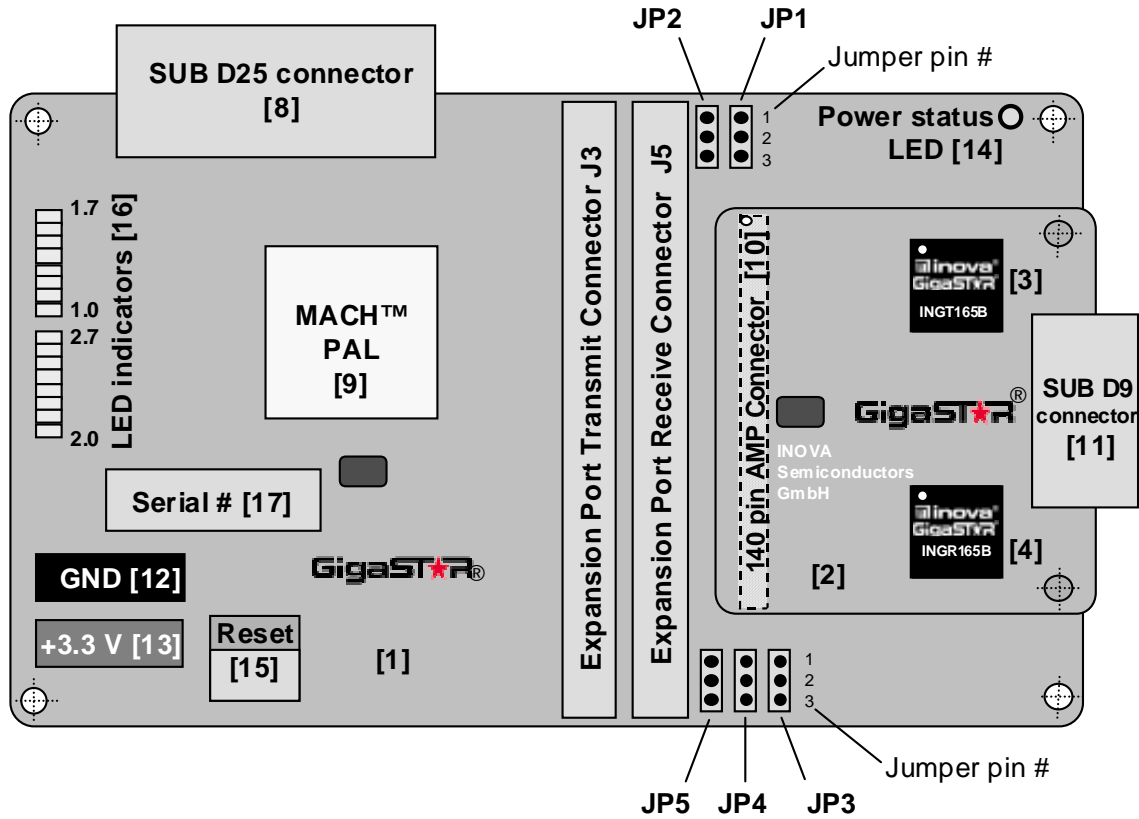


Figure 1 : Application Kit main board with mounted Piggyback Board

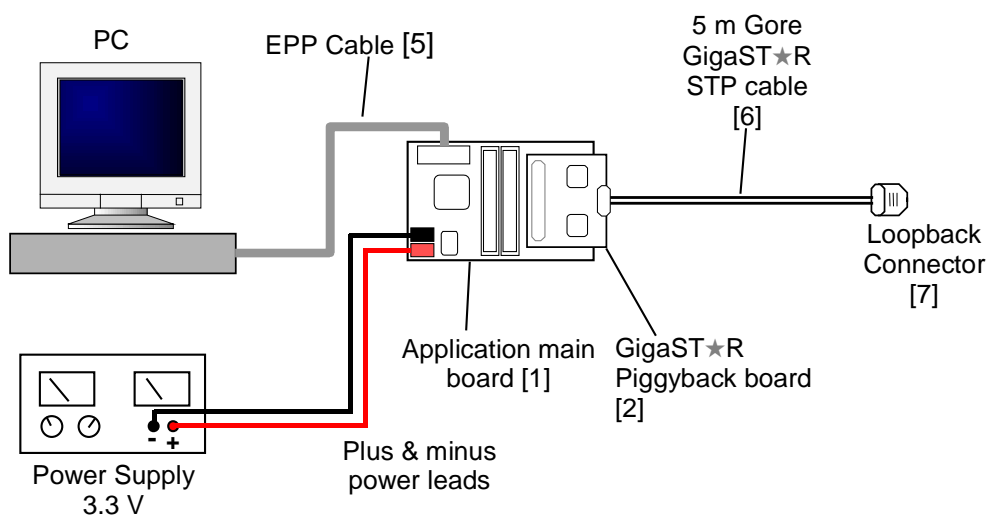


Figure 2 : Application Kit startup configuration with Loopback Connector

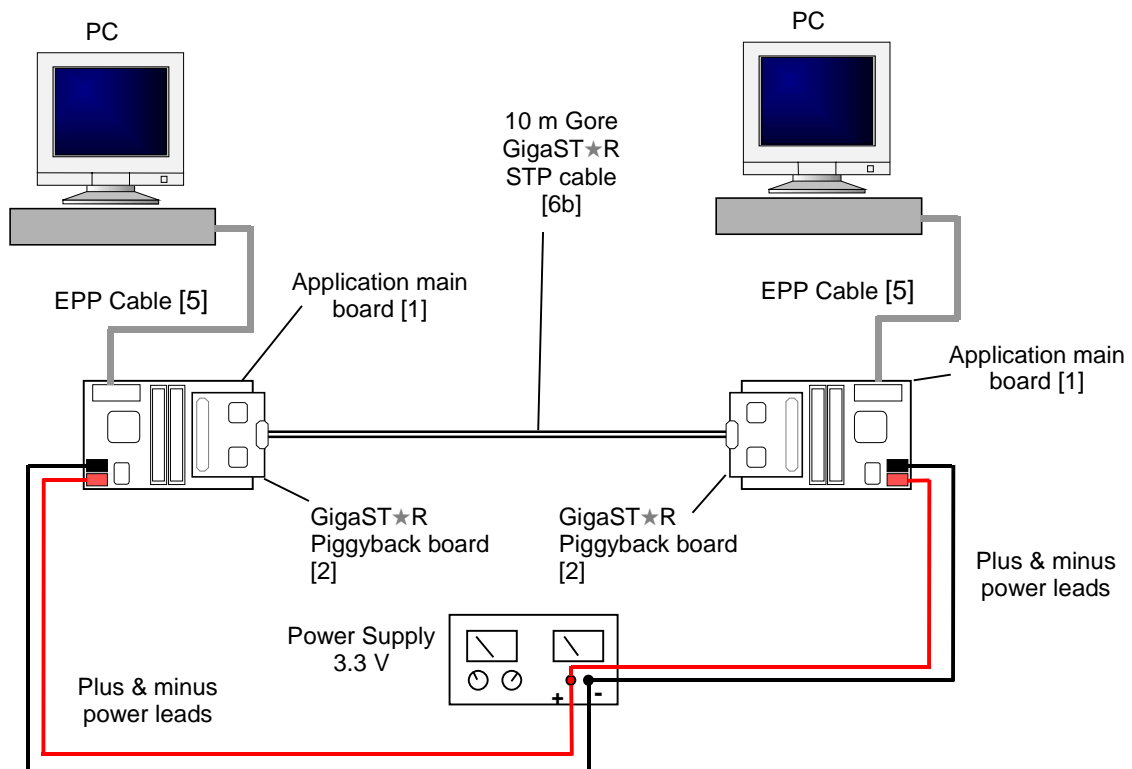


Figure 3 : Application Twin Kit duplex configuration

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1 Introduction

The GigaSTaR Application Kit is a versatile and modular tool to easily build up a fully operational 1.32 Gbit/s high-speed GigaSTaR link to either adapt it to any existing system environment or to evaluate the link under specific and predefined conditions. It provides the user with a plug-and-play environment supporting a step by step integration of the GigaSTaR link into the customers target application.

The enclosed software offers a variety of operation modes like to download data, to read and display transmitted data and to configure and control the bench setup.

Any data can be directly loaded into the transmit FIFOs on the Application Board via a parallel data interface (EPP-port). Vice versa, also the received data can be accessed the same way through the receive FIFOs of the application board.

While the access to the FIFO buffers via the EPP-port is limited to the speed of this parallel interface, the direct access to the data buffers via the Expansion ports allows to transfer data with no bandwidth limitations up to the maximum data rate of the GigaSTaR link.

For technical details and parameters of the boards and the GigaSTaR products see the product data sheets, the actual revisions are available as pdf-files on the Inova Semiconductors Web-page: <http://www.inova-semiconductors.com>.

1.1 Application Kit Configuration

The Application Kit contains two printed circuit boards, the application main board [1] and the mounted GigaSTaR Piggyback board [2] with the GigaSTaR Transmitter [3] and Receiver devices [4] (*figure 1*). The kit further encloses a parallel interface cable [5], a 5m Shielded Twisted Pair (STP) high-speed serial cable (*GORE #GGSC1608-5*) [6], a loopback connector [7] and a CD-ROM with the application kit software and all product datasheets (*figure 2*).

The GigaSTaR application main board [1] is equipped with a parallel-port connector [8] to interface to a PC with the enclosed parallel cable [5]. The on-board MACH™ PAL [9] handles the EPP port protocol as well as the transmit- and receive- data buffer control.

The Piggyback board [2] communicates to the application main board [1] via two each 36 bit wide transmitter and receiver parallel data interfaces and is plugged to the Application Main Board with a 140-pin AMP free-height connector [10]. The mounted SUB D9 connector [11] is a receptacle to directly plug in the enclosed STP cable [6].

For detailed technical information on the Piggyback board see the datasheet.

The GigaSTaR Application Twin Kit contains two Application Kits plus a 10m Shielded Twisted Pair (STP) high-speed serial cable (*GORE #GGSC1608-10*) [6b] to directly connect the two printed circuit boards.

1.2 User Registration

Registered users of the application kit automatically will be notified about new software releases, technical changes of the application kit, new application notes or other changes. To register, send an email to: gsapp@inova-semiconductors.de, containing the user name, address and the serial number [17] of the application board.

2 Technical Description

2.1 Application Main Board Interfaces

The application main board provides 4 interfaces to peripheral devices and systems:

- the EPP connector [8] to interface to a PC
- the AMP 140 pin connector [10] interfacing to the Piggyback board
- the 64 pin ribbon cable Expansion Port connector [J3] for direct access to the Transmitter FIFOs at full bandwidth
- the 64 pin ribbon cable Expansion Port connector [J5] for direct access to the Receiver FIFOs at full bandwidth

Note: Detailed pin assignments of the connectors and signal timing diagrams can be found in the application kit data sheet ING_AK_DS.

2.2 Data path and control signal configuration

2.2.1 Transmit Data Path

Transmit data provided by the MACH™ PAL [9] or via the Expansion Port connector [J3] are loaded into the 512 x 36 Bit transmit FIFO buffer. Once the data valid signal is asserted to the the GigaSTaR transmitter, it starts to load the data from the FIFO, serialize it and sends the data out to the shielded twisted pair cable.

The MACH™ PAL [9] extends the data path to enable two different operation modes:

Repeated burst transmission : The Tx-FIFO is continuously re-loaded with identical data while its buffer content is transmitted to the TX device. In this mode, identical data words are transmitted over the STP cable until the transmission is stopped. Bit errors will not accumulate.

Tx-Rx Loopback : This mode is possible by using the loopback plug configuration as shown in figure 2. The data which are transmitted from the Tx-FIFO over the Link to the Rx-FIFO are circulated back to the Tx-FIFO forming a closed loop data transmission. Eventually occurring bit errors will accumulate over time. The bit error rate can be calculated by comparing the original data sequence with the data sequence maintained in the Rx-FIFO.

(see also 4.1.2 “Transmit data Entry”, page 18, and 4.1.3 “Transmission modes”, page 19)

2.2.2 Receive Data Path

Serial data received at the Receiver [4] are converted back to 36 bit wide parallel data. These data are clocked into the receive FIFO. Received data can be accessed via the EPP connector [8] through the MACH™ PAL [9] or directly at the Expansion Port connector [J5].

2.2.3 Clock System and Reset

The application main board [1] provides a power up reset to initialize the hardware correctly.

An on-board oscillator provides a 66 MHz clock. This clock is divided by 2 for the application main board system clock. The Piggyback board [2] operates with its own 66 MHz reference clock.

2.2.4 Flag Insertion

The GigaSTaR link features a mechanism to transmit side band signaling information, a so- called flag. The main intention of the flag signal is to mark the data word, which is currently transmitted. This allows adding frame information to a data burst. To flag a specific data word requires to store the flag information in the FIFO in parallel with the data. For this purpose the Transmitter flag signal (FLAGI) can be assigned via jumpers to the data bit 34 of the transmit FIFO. At the receiving side the bit 34 of the Rx-FIFO can be assigned via jumpers to the Receiver flag signal (FLAGO).

2.2.5 Parity Generation

The Transmitter is able to generate a parity bit. If the PARGEN mode is enabled this parity bit is generated automatically. If the PARGEN mode is disabled, the parity bit has to be supplied externally, otherwise the receiver indicates parity errors. As the FIFOs only support 36-bit wide data, the Transmitter parity signal (TX_PARITY) can be assigned to the data bit 35 of the transmit FIFO, the same for the Receiver parity signal (RX_PARITY) at the receiving side.

(see 2.2.6 “Jumper Settings”)

2.2.6 Jumper Settings

The purpose of the jumpers (JP1 to JP4) is to demonstrate the “FLAG” and “PARITY” features despite of the limitation of the FIFO’s parallel bus to 36 bit: The data path can be modified in a way that the FLAGI / FLAGO and the TX_PARITY/RX_PARITY signals either are directly routed to the MACH™ PAL [9] and the Expansion Port connectors [J3], [J5] or are assigned to bit 34/35 of the transmitted data word and stored in the FIFO (default settings).

Jumper	Connection Pin 1 & 2 (default setting)	Connection Pin 2 & 3
JP1	MACH™[FLAGI] -> GigaSTAR®[FLAGI] MACH™[TXFD34] -> FIFO[D34]	MACH™[FLAGI] -> FIFO[D34] -> GigaSTAR®[FLAGI]
JP2	MACH™[TXPARITY] -> GigaSTAR®[TX_PARITY] MACH™[TXFD35] -> FIFO[D35]	MACH™[TXPARITY]->FIFO[D35]- >GigaSTAR®[TX_PARITY]
JP3	GigaSTAR®[FLAGO] -> MACH™[FLAGO] FIFO[D34] -> MACH™[RXFQ34]	GigaSTAR®[FLAGO] -> FIFO[D34] -> MACH™[FLAGO]
JP4	GigaSTAR®[RX_PARITY] -> MACH™[RXPARITY] FIFO[D35] -> MACH™[RXFQ35]	GigaSTAR®[RX_PARITY] -> FIFO[D35] -> MACH™[RXPARITY]
JP5	Has to be set on this position permanently	Reserved for optional functionality

Table 1: Jumper Settings of Application Main Board

2.2.7 LED Array

The 2 x 8 Bit LED Array [16] informs about the actual settings of the Application Kit (Equalizer on/off, Parity, Flag), the selected operation mode (Loopback, Single- & Repeated Bursts, Expansion Port), the status of the FIFO buffers and occurring transmission errors (PLL unlock, Frame- and Parity Error):

LED #	Function	Code	LED #	Function	Code
1.7	Rx Equalizer selected	EQL	2.7	Rx FLAGO	RFG
1.6	---		2.6	Rx Frame Error	LSY
1.5	Tx PARGEN enabled	PAG	2.5	Rx PLL Unlock	ULK
1.4	Tx-Rx Loopback	CYG	2.4	Rx FIFO full	RFL
1.3	Tx Repeated Burst	RPB	2.3	Rx FIFO empty	REY
1.2	Tx Single Burst	SGB	2.2	Tx Parity Error	PER
1.1	Tx Single Word	SGW	2.1	Tx FIFO full	TFL
1.0	Expansion Port enabled	EXP	2.0	Tx FIFO empty	TEY

Table 2: LED Array information

2.3 DC Power Supply

The board operates from a single 3.3 V DC power supply. The typical current consumption per set of boards is 1A .

Both, the application main boards and the piggyback boards don't have any measures against overvoltage or reverse polarity, therefore the connections and settings should be checked carefully.

For reproducible evaluations and measurements it also is recommended to use a quality power supply with good stability and adequate filtering against transients and RF-noise.

2.4 Block Diagram of the Application Main Board

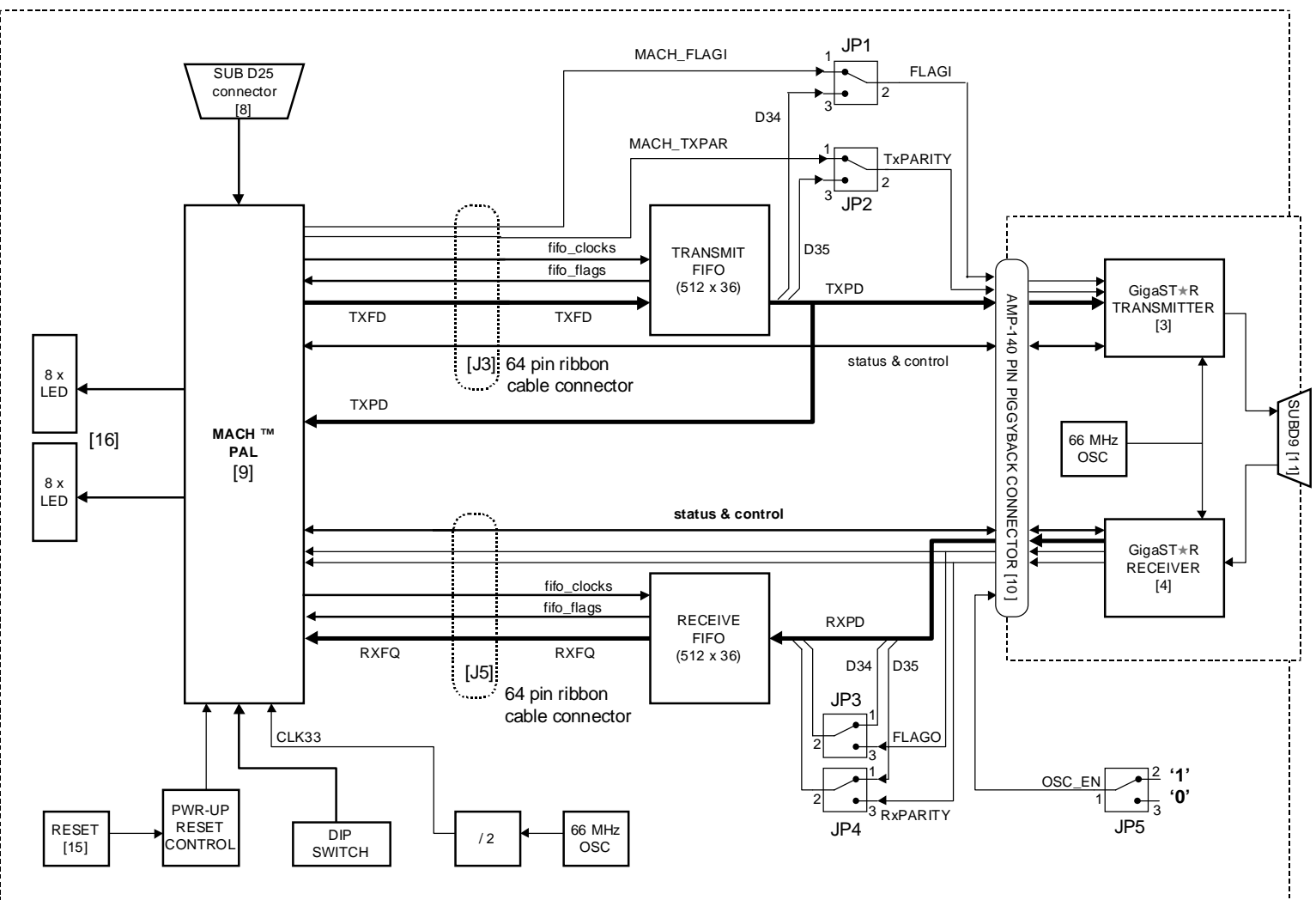


Figure 4: Application Kit Main Board Block diagram

3 Getting started

3.1 Application Kit Software License Agreement

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3.2 System Requirements

- IBM compatible PC with VGA display, Floppy, CD-ROM and a parallel port capable to operate in EPP mode.
- DC power supply capable to provide 3.3 V @ 1 A (see also 2.3 "Power Supply", page 8)

The parallel printer port has to set to "EPP mode". The PC's motherboard manual usually contains the BIOS settings (Preferably EPP1.9 over EPP1.7 over EPP/ECP). The base address of the parallel port is required (0x378, 0x278, 0x3BC are supported), The software's default setting is (0x378)

The application kit software on the CD-ROM can be invoked directly from any DOS operating platform with CD-ROM support or can be started under Windows 95/98. Using Windows 95/98 will limit the real time capabilities of the software.

If real time operation is desired or if DOS / Windows 95/98 is not available, a bootable DOS floppy can be created , an image for such a floppy is on the CD-ROM. The floppy disk boots FreeDOS and contains all software required to run the application kit. Note: CD-ROM access is not supported in this mode.

3.3 Steps to create a bootable floppy disk

1. Insert the application kit CD-ROM
2. Open a DOS Command Shell
3. Change to directory \software\bin on the CD-ROM drive
4. Insert an empty floppy disk (1.44 MB)
5. Type (assuming the floppy disc drive is a: and CD-ROM drive d: is used) :
 - *For Windows NT :*
ntrw d:\disk\fdimage a: <return>
 - *For DOS / WIN95 / WIN98 :*
rawrite -f d:\disk\fdimage -d a: <return>

3.4 Powering Up

The instructions below refer to the figures 1,2 and 3

1. Connect the 5m STP-cable [6] (Application Twin Kit : 10m cable [6b]) with the SUB - D9 Connector [11].
2. Plug and lock the loopback connector [7] to the other end of the STP- cable [6] (single Application Kit only).
3. Connect the parallel interface cable [5] to the EPP connector [8] and the parallel port of the PC.
4. Connect the (-) power lead (not included in the Application Kit) to the black ("GND") connector [12] of the application main board [1] and to the (-) terminal of the power supply.
5. Connect the (+) power lead (not included in the Application Kit) to the red ("+3.3 V") power connector [13] of the application main board [1] - Do not connect yet the (+) power lead to the (+) terminal of the supply !
6. Switch on the power supply.
7. Set the voltage to 3.3 V DC (+/- 5%).
8. **Double check polarity and voltage, there is no over-voltage or reverse polarity protection on board !**
9. Plug in the (+) power lead to the (+) terminal of the power supply. The power status LED [14] should turn on.
10. Press the reset button [15] on the application main board.

3.5 Starting the Software

3.5.1 Starting from CD-ROM

1. Turn on and boot the PC
2. Insert the CD-ROM
3. Change to the CD-ROM drive directory
4. Change to \software\bin directory
5. On the command line type:

gigastar <CD-ROM drive> [port address] <return>

Note : the port address is an optional information, if no port address is entered, the default port address [0x378] will be used.

Remarks :

Example 1: **gigastar G <return>** *CD-ROM is G; port base address is 0x378*

Example 2: **gigastar F 0x278 <return>** *CD-ROM is F; port base address is 0x278*

3.5.2 Starting from Boot Floppy Disc

1. Insert boot floppy disc (see also 3.3) and turn-on the PC
2. On the command line type:

gigastar <floppy drive> [port address] <return>

Note : the port address is an optional information, if no port address is entered, the default port address [0x378] will be used.

Remarks :

Example 1: **gigastar A <return>** *Floppy drive is A; port base address is 0x378*

Example 2: **gigastar B 0x278 <return>** *Floppy drive is B; port base address is 0x278*

4 Data Transmission

4.1 PC Software Interface

Note : Some operating modes are restricted to the loopback configuration with a single application board.

4.1.1 Main Menu

The software provides a Graphical User Interface (GUI) which allows the user to separately control the 4 main function blocks of the application kit:

The Tx-FIFO [1], the Transmitter [2] and Receiver device [3] and the Rx-FIFO [4].

Each of the blocks is controllable by a separate menu which can be selected by pressing the numeric keys 1-4 on the PC keyboard.

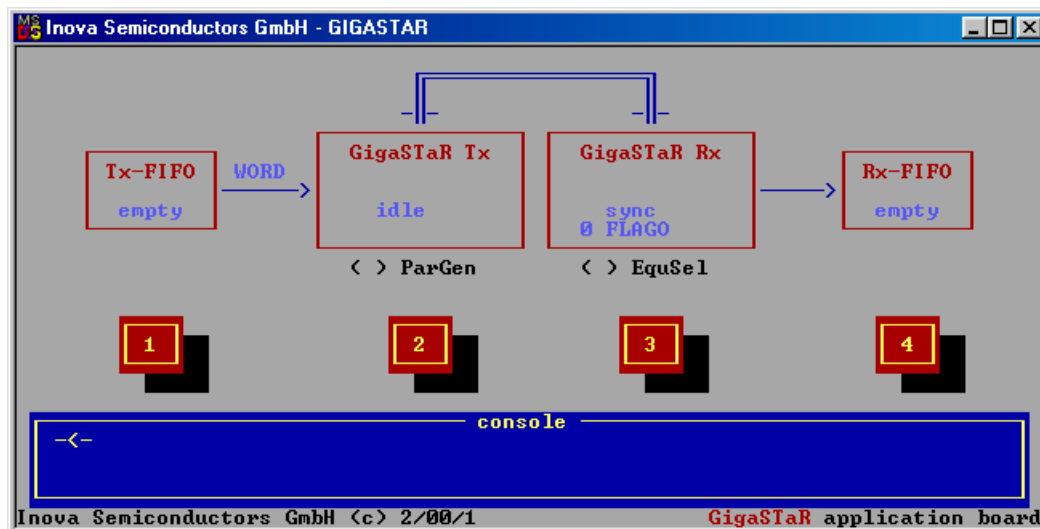


Figure 5: Software Main Menu

To leave an activated menu, press ESC. To exit the program press "SHIFT Q", after deactivating all menus.

If a selection is displayed in square brackets [], it means that this is the default value for this entry field which can be accepted by pressing the RETURN key.

The Application Kit uses the loopback principle for all the transmission modes to realize a complete transmission system with only one set of boards.

The transmitter (Tx) device is sending out the serial data stream to pins 1, 6 (Tx+, Tx-) of the STP cable [6] which contains two pairs of shielded twisted copper wires. The loopback connector [7] at the loose end of the STP-cable simply connects the "transmit" pair with the "receive" pair thus returning the signal back to the Receiver (Rx) device on pins 5,9 (Rx+,Rx-). This finally is doubling the distance the signal has to travel, the enclosed 5 m STP cable [6] thus represents a transmission distance of 10 meters.

The Tx-Rx-Loopback mode implements a loop from the Tx-FIFO via the Link to the Rx-FIFO back to the input of the Tx-FIFO. Data loaded in the Tx-FIFO are transmitted to the Rx-FIFO until the Tx-FIFO is almost empty. Now the received data are written from the Rx-FIFO back to the Tx-FIFO. Pressing key '3' will stop the transmission.

This mechanism allows to read out almost all data of the Rx-FIFO which were transmitted in loopback mode after the transmission was interrupted either by the 'stop' button or by a transmission error such as the lost of frame synchronization. Almost all data means that approximately 7-8 words will be lost in the loop due to the cable delay time (approx. 4ns/m)

In this configuration, special loopback software modes are available to monitor the bit error rate of an application board (see 2.1.3.).

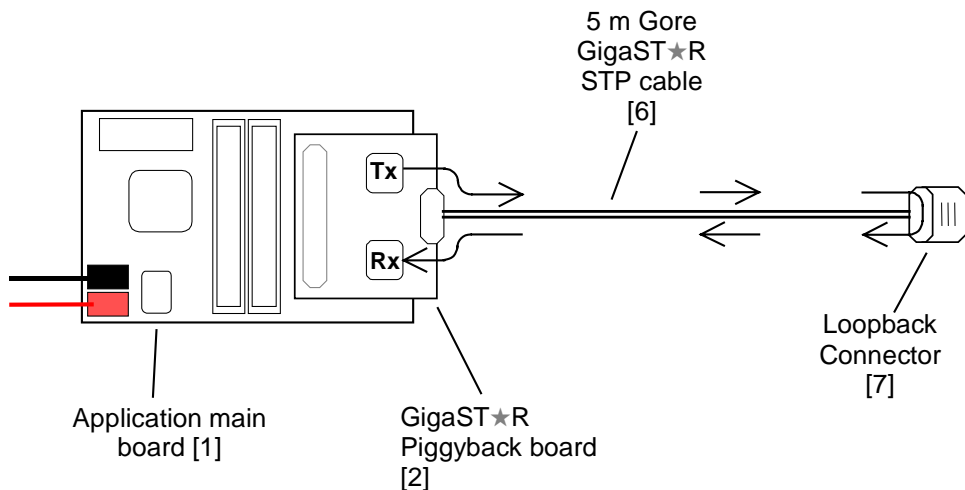


Figure 6: Single Application Kit data flow using the loopback connector

With the Application Twin Kit a true full duplex transmission with a datarate of $2 \times 1.32\text{Gbit/s}$ can be established between the two boards (see figure 7). The features of the loopback setup (see above) are not available in this operation mode.

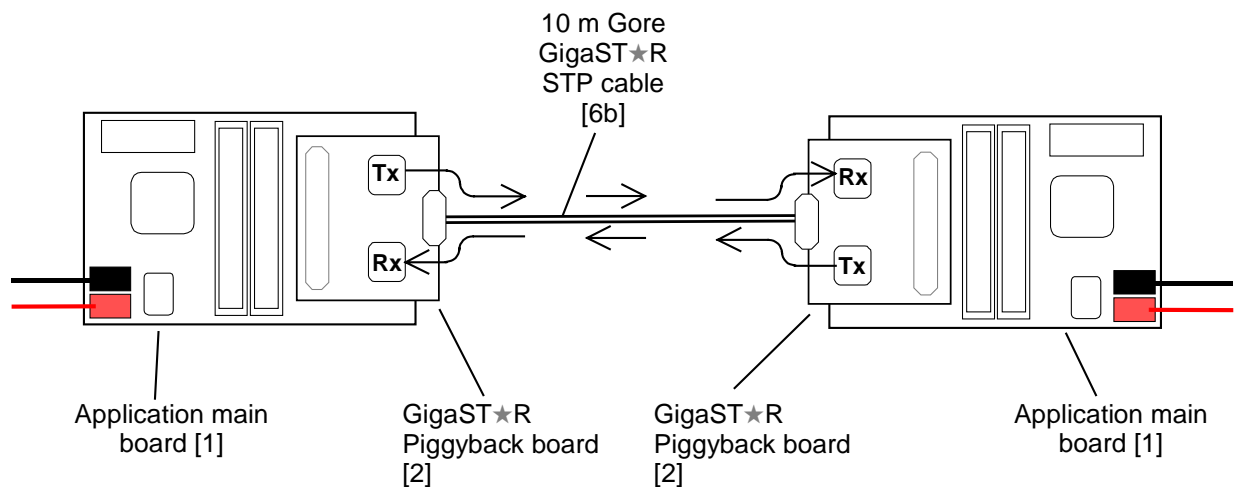


Figure 7: Application Twin Kit data flow (full duplex) using two Application Boards

Menu (1) : Tx FIFO

In this menu (selection by pressing '1') the transmit data can be stored in the Tx-FIFO buffer. The data can be entered manually pattern by pattern by selecting submenu '2' ('Write'). Activating the submenu 'Fill' (press '3'), a variety of predefined data pattern is available to choose from.

(For details on the data entry see also 4.1.2 "Transmit Data Entry").

Pressing '1' resets the TxFIFO. When the software starts up, all devices are reset automatically, so no manual start-up reset of the four devices is required.

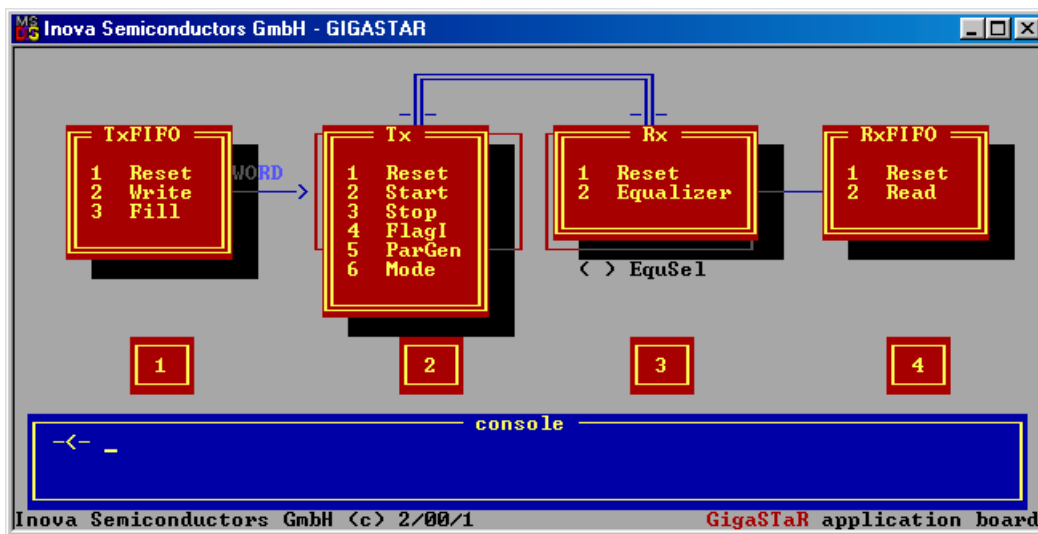


Figure 8: Submenus of the function blocks (1) to (4)

Menu (2) : Tx Device

This menu controls the Tx device. Pressing the '1' key resets the Tx device. By selecting '2' for 'Start', the content of the Tx-FIFO is sent out by the transmitter device. Selecting '3' will stop a running transmission. Choosing '4' activates the 'FLAGI' function inserting a flag into the transmitted data. The reception of the flag is displayed at the Rx block, the 'FLAGO' value will toggle from 0 to 1 or vice versa.

(see 2.2.6 'Jumper Settings' and the data sheet for details on the FLAGI/FLAGO routine).

Choosing '5' activates the internal parity generator (the LED 'PAG' in the LED array [16] will turn on). This ParGen Function should be always activated unless a parity bit is correctly provided through the expansion port. Choosing '6' opens a further submenu allowing to choose from several transmission modes (see 4.1.3 "Transmit Modes")

Menu (3) : Rx Device

Similar as for the Tx device, pressing the '1' key resets the Rx device. Depending on the type and length of the used STP cable, an integrated impedance Equalizer can be activated by pressing '2' (the LED 'EQL' in the LED array [16] will turn on). For the enclosed 5m STP cable [6] in loop-back mode (corresponding to 10 m distance) as well as for the Twin Kit 10m STP cable [6b] directly connecting the two sets of boards, the Equalizer should be activated. For other STP-cables of different type or length the setting of the Equalizer may differ.

Menu (4) : RxFIFO

The received data is available at the Rx-FIFO buffer. Selecting submenu point '2', the data received by the Rx device are being displayed. Pressing '1' resets the Rx device.

4.1.2 Transmit Data Entry (TxFIFO Menu)

Menu (2) "Write"

Transmit data can be entered manually in hex code on a word by word basis. Each word consists of 8 hex code characters thus representing 32 bit. Data up to a maximum of 512 words can be entered in the TxFIFO. To stop data entry and exit the data entry, press 'q' and then the RETURN key. Please do not press the escape key to exit, this will stall the program.

Menu (3) "Fill"

A more convenient way to fill the TxFIFO is to use predefined data sequences. The software offers a variety of patterns including pseudo random or alternating bit sequences. The patterns can be selected by the keys '1 – 7' Note: The download of the patterns into the TxFIFO may take a couple of seconds. Choosing '8' for 'special load' will start a special manual data entry routine, which provides special routines like "repeat" (the entered data words will be repeated as many times as the number entered) and "invert" (each data word will be followed by its inverted value, the total number of words transmitted will not change). To exit the data entry field, press 'q' and then the RETURN key. Please do not press the escape key to exit, this will stall the program.

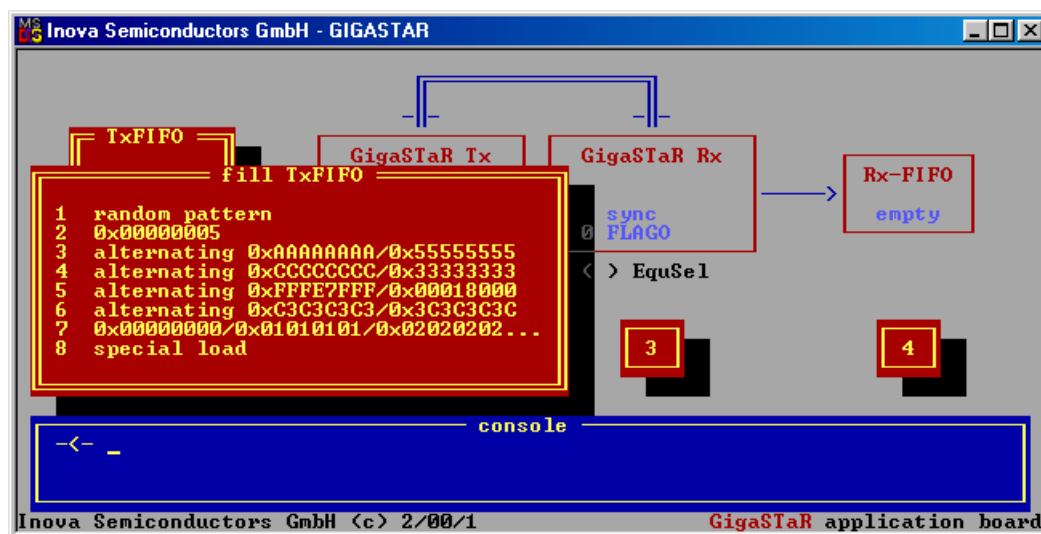


Figure 9: Tx FIFO Menu "Fill" options

4.1.3 Transmission Modes (Tx Device Menu)

Menu (6) "Mode"

Four different transmission modes are offered by the software and can be selected by pressing keys '1' - '4'. In addition a macro function is integrated, which allows a type of automated bit error test using a PRBS-signal (key 'B').

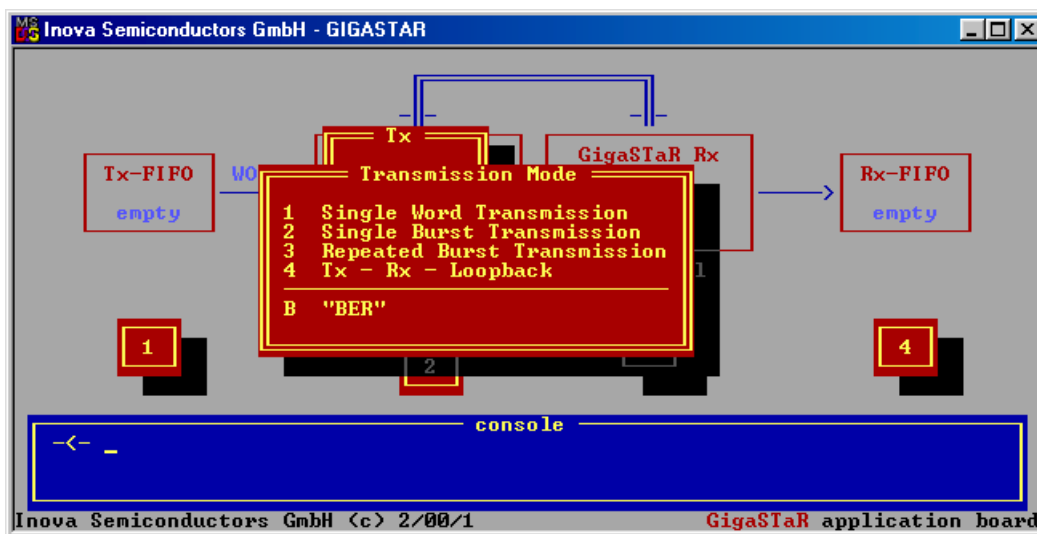


Figure 10: Tx Device Menu "Transmission mode"

Submenu (1) "Single Word Transmission"

In the Single Word Transmission mode one word is read out of the Tx-FIFO and transmitted over the Link to the Rx-FIFO once the 'start' button is pressed. This is the default mode if no other mode is selected. After each write cycle at the TxFIFO respectively read cycle at the RxFIFO, the transmission mode is set back to the default mode "single word transmission".

Submenu (2) "Single Burst Transmission"

In the Single Burst Transmission mode data is read out of the Tx-FIFO until the Tx-FIFO is empty. The data are transmitted over the link to the Rx-FIFO once the 'start' menu is activated (key '2').

Submenu (3) "Repeated Burst Transmission"

During the Repeated Burst Transmission mode the output data of the Tx-FIFO are permanently looped back to its input register. The result is a repeated burst sequence of the data words previously stored in the Tx-FIFO. The transmission can be halted by pressing key '3' (Stop).

Submenu (4) “Tx-Rx-Loopback” (available for loopback configuration as shown in figure 6)

The Tx-Rx-Loopback mode implements a loop from the Tx-FIFO via the Link to the Rx-FIFO back to the input of the Tx-FIFO. Data loaded in the Tx-FIFO are transmitted to the Rx-FIFO until the Tx-FIFO is almost empty. Now the received data are written from the Rx-FIFO back to the Tx-FIFO. Pressing key ‘3’ the transmission can be stopped.

This mechanism allows to read out almost all data of the Rx-FIFO which were transmitted in loopback mode after the transmission was interrupted either by the ‘stop’ button or by a transmission error such as the lost of frame synchronization. Almost all data means that approximately 7-8 words will be lost in the loop due to the cable delay time (approx. 4ns/m).

Submenu option (B) “BER” (available for loopback configuration as shown in figure 6)

In this mode, the Bit Error Rate (BER) macro fills the Tx-FIFO with a sequence of 512 pseudo random bit sequence (PRBS). Any other data previously written into the Tx-FIFO will be overwritten and ‘ParGen’ is automatically selected.

This operation mode does not affect the equalizer, please verify its correct settings before starting the Bit Error Test. After selecting ‘B’ in the Tx Device Menu, the PRBS data are transmitted in the Loopback Mode. The time between the start of the transmission and the occurrence of a bit error or a loss of frame synchronization is used to calculate the Bit Error Rate. The average, minimum and maximum times between the occurrence of a bit errors or loss of frame synchronizations are calculated and displayed on the screen (see figure 9). This mode is running continuously until it is halted by pressing any key.

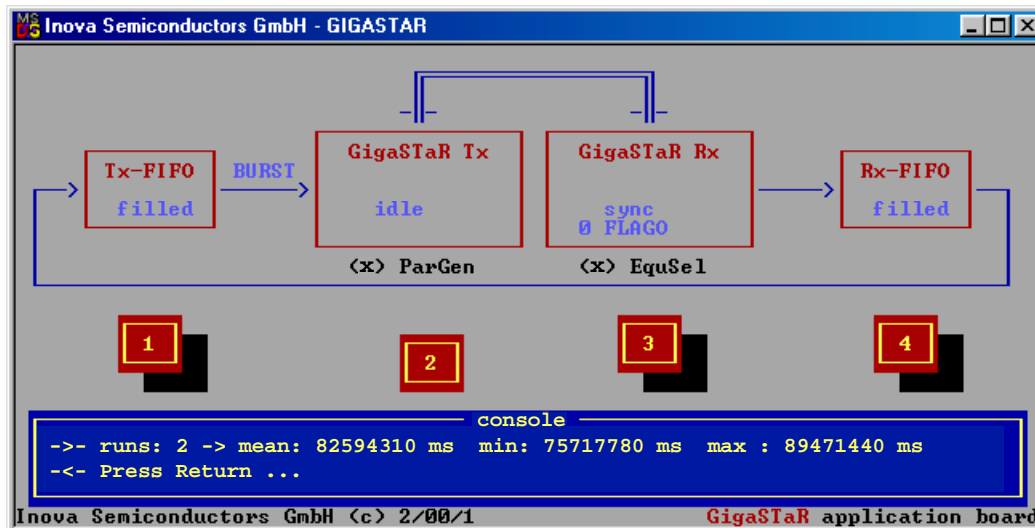


Figure 11: Transmission mode ‘BER’ screen display with bit error measurement results

4.1.4 Receiving Data

The serialized data are received by the Rx-Device and stores in the Rx-FIFO. The synchronization status and the actual value of the ‘FLAGO’ signal are recorded and displayed in the Rx box. Selecting ‘2’ in the Rx-FIFO menu displays the received data with the option to select the number of words shown.

Data words which have been read out of the Rx-FIFO buffer get automatically erased.

4.2 Expansion Port

Besides the software controlled operation of the Application Kit via the EPP port [8], also direct access to the transmit- and receive buffers is provided. All control- and status signals required to write data in the transmit buffer (Tx-FIFO) or to read out data of the receive buffer (Rx-FIFO), are available at the two 64 pin ribbon cable Expansion port connectors [J3] and [J5] (see figure 1).

The pinout of the Expansion port connectors [J3] and [J5] can be found in the application board data sheet "ING_AK_DS".

This setup enables data transmissions from and to the user application up to the maximum speed of the GigaSTaR link (1.32 Gbit/s).

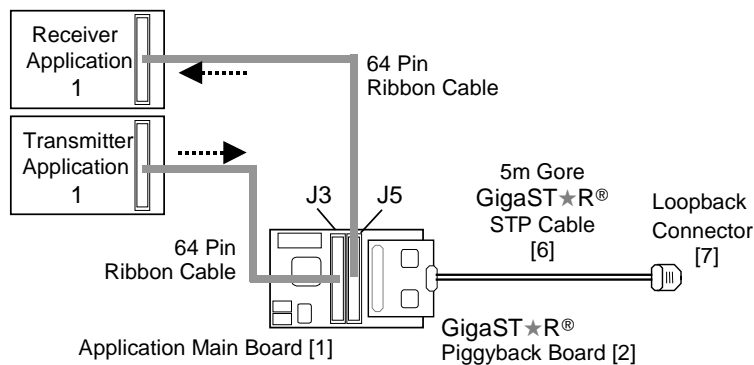


Figure 12: Application Kit Loopback configuration using the Expansion Ports

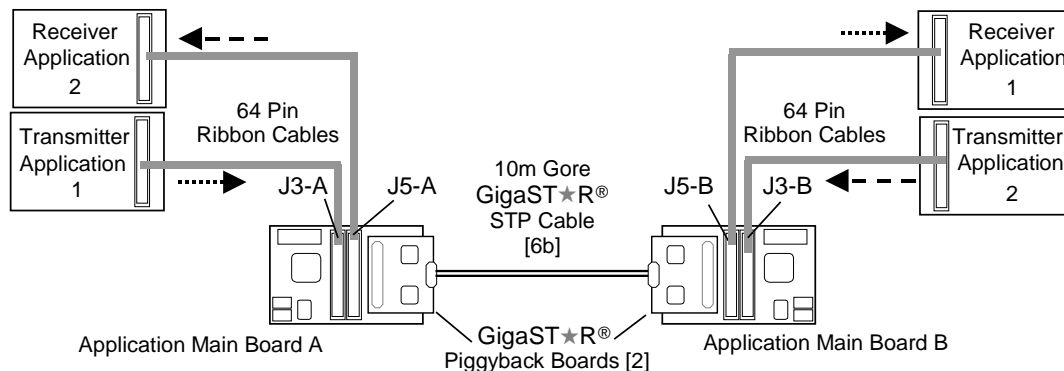


Figure 13: Application Twin Kit full duplex configuration using the Expansion Ports linking Port J3-A with Port J5-B and Port J3-B with Port J5-A

5 Handling Precautions

Handling precautions are:

1. The application kit boards do not contain any protection against overvoltage and reverse supply polarity, please check the voltage and polarity carefully before connecting the boards.
2. The maximum ratings of the components (see datasheets “ING_AK_DS” and “ING_TRC_DS”) may not be exceeded at any time.
3. Precautions have to be taken against exposure of board terminals to electrostatic discharge stress.
4. The application kit boards have been designed for the purpose of electrical evaluation in an engineering environment and does not have any EME/EMI-provisions. If the boards are used in an EME/EMI-sensitive environment, extra shielding measures may be necessary.
5. Mounting and dismounting of the Piggyback boards should be performed with care. These dis/mounting cycles should be limited in order to avoid wearout of the 140 pin fine-pitch connector.

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