

2.64 Gbit/s Serial Link Piggyback Board

The GigaSTaR piggyback boards ING_TTC and ING_RRC represent an easy-to-use implementation of a dual GigaSTaR High-Speed link with 2.64 Gbit/s (330 Mbyte/s) bandwidth. Equipped with 2 GigaSTaR INGT165B Transmitter devices (ING_TTC) or 2 INGR165B Receiver devices (ING_RRC) plus external components, the boards offer all the functionality to be directly connected to a plain 2x36bit, 33 MHz parallel Interface through a compact 140 pin connector. The high-speed serial signals are available at a SUB D9 connector which is directly mounted on the piggyback board. The pinout is compatible to industry-standard Shielded-Twisted-Pair (STP) cables. With the compact size of 64 x 59 mm and a variable distance of 6-14 mm to the main board, this piggyback can be easily adapted to any system environment.

The GigaSTaR piggyback boards are also available as full-duplex version ING_TRC. For information on the piggyback board with fiber-optic interface see the ING_TRF datasheet. Technical details on the GigaSTaR Transmitter- and Receiver-devices INGT165B/INGR165B are available in the product datasheet ING165B_DS.

GigaSTAR[®] Piggyback Boards ING_TTC/RRC

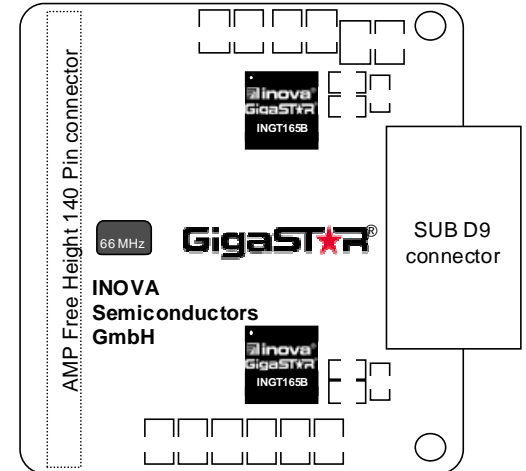


Figure 2: Original size of the piggyback board

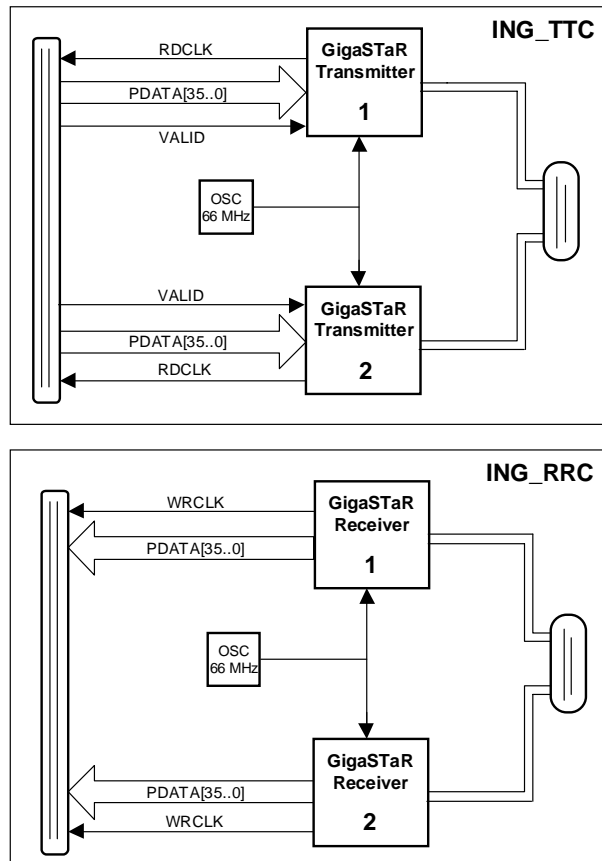


Figure 1: Piggyback Board ING_TTC/RRC functional schematics

FEATURES

- Compact size of 64 x 59 mm
- 297 Mbyte/s payload data rate (sustained)
- Parallel Interfaces 2x36 bit @ 33 MHz)
- Mounted SUB D9 receptacle for connection to Shielded Twisted Pair Cable (Gore part #:GGSC1608-X)
- 140 pin, 0.8 mm pitch Free-Height Connector (AMP part #179029-6 for selectable height receptacles : 6/10/14 mm board spacing)
- On-board reference-clock (prepared for optional external clock)
- Full AC-coupling to the serial link cable (100nF, 50 V capacitors)
- Multi-layer board for highest EMI-immunity
- Single 3.3 V DC-supply

1. GigaSTaR LINK DESCRIPTION

The GigaSTaR link is designed for reliable high-speed low-latency data transmissions. All functions for the data transfer management including the high-frequency blocks are fully integrated in the GigaSTaR Transmitter and Receiver devices. Each device features a 36-bit “user-friendly” parallel interface with standard logic levels (3.3V CMOS) for easy adaptation to any application.

The ING_TTC/RRC piggyboards allow to set up two independent GigaSTaR links with a total sustained payload data rate of 297 Mbyte/s. Each link supports an effective (sustained) data rate up to 148.5 MByte/s at the parallel interface, which translates to a serial bit stream of max. 1.188 Gbit/s (payload data rate). With 4 additional bits for link-synchronization, DC-balancing and parity check the maximum bit rate at the serial I/Os is 1.32Gbit/s per link, for an overall link efficiency of 90 percent. With only 40 ns propagation delay time each for the Transmitter and Receiver, the typical overall latency for a GigaSTaR link is:

$$\text{latency [ns]} = 2 * 40 \text{ ns} + 4\text{ns/m} * \text{cable-length [m]}$$

For example, the latency is about 160 ns for a 20 meter connection with Shielded-Twisted-Pair (STP) copper cable.

Note:

For all timings and descriptions of the ING_TTC piggyback board, timing names beginning with TX1/2 indicate that this timing parameter is valid for the transmitter device #1 as well as transmitter device #2.

For all timings and descriptions of the ING_RRC piggyback board, timing names beginning with RX1/2 indicate that this timing parameter is valid for the receiver device #1 as well as receiver device #2.

1.1 CLOCK SYSTEM

The serial bit clock frequency of 1320 MHz is generated by internal PLLs. The Transmitter and Receiver each require an external 66 MHz reference clock.

A continuous phase alignment in the Receiver ensures that the receive clock is synchronous to the transmit clock.

1.2 PARALLEL DATA FORMAT

Each GigaSTaR Transmitter and Receiver device features a synchronous 36 bit parallel interface. As the ING_TTC and ING_RRC piggyback boards feature 2 transmitter respectively receiver devices per board, the parallel interface of the boards is 2*36 Bit wide. The maximum frequency at this interface is 33 MHz, equivalent to a period of 30.3 ns for the RX1/2_WRCLK and TX1/2_RDCLK signals.

The TX1/2_PARGEN input pin controls the transfer of the optional external parity bit synchronous with the parallel data. If an external parity bit is provided by the application at the TX1/2_PARITY input pin, TX1/2_PARGEN has to be set to '0'. The Transmitter will read in the external parity bit at the TX1/2_PARITY pin and will compare it with the parity bit generated internally. The TX1/2_PERR# signal reports any mismatch between the external parity bit and the internally generated parity bit.

If no external parity bit is available, TX1/2_PARGEN has to be set to '1' and the Transmitter adds the internally generated parity bit to the data word. The TX1/2_PERR# signal is inactive when TX1/2_PARGEN = '1'.

The Receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of both parity information indicates a transmission failure and the signal RX1/2_PERR# is asserted for one data cycle. RX1/2_LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

1.3 SERIAL DATA FORMAT

The serial data stream is DC-balanced to support capacitive (AC) coupling for full DC isolation of the link. This is performed by proprietary coding in the Transmitter device.

1.4 TRANSMITTER CONTROL SIGNALS (ING_TTC)

TX1/2_RESET# is an asynchronous active low reset signal for the Transmitter device.

TX1/2_PARITY is the input pin for the externally provided parity signal.

TX1/2_PERR = '1' indicates that the externally provided parity bit does not match the internally generated parity bit.

TX1/2_LOCK = '1' indicates that the Transmitter PLL is locked. If TX1/2_LOCK is de-asserted the Transmitter is not ready.

TX1/2_PARGEN = '1' activates the internal parity generation. In this mode, the PARITY input pin is ignored. An internal parity bit is generated and transmitted.

TX1/2_VALID = '1' indicates to the Transmitter that data are available. With the assertion of TX1/2_VALID the TX1/2_RDCLK starts to run. TX1/2_PDATA[35..0] is registered at each rising edge of TX1/2_RDCLK. De-asserting TX1/2_VALID disables TX1/2_RDCLK and stuffing patterns are transmitted over the GigaSTaR link to maintain synchronization.

A TX1/2_FLAGI positive edge sets an internal flag which is inserted at the end of the data word currently in transmission. The Receiver decodes the flag out of the serial bit-stream and toggles the level of the RX1/2_FLAGO output. This signal can be used to mark the end of a data frame.

1.5 RECEIVER CONTROL SIGNALS (ING_RRC)

RX1/2_RESET# is an asynchronous active low reset signal for the Receiver device.

RX1/2_PARITY is the output pin for the parity bit transmitted with the 36 bit data word.

RX1/2_PERR# is asserted for one data cycle if a mismatch of the transmitted and internally generated parity information indicates a transmission failure.

RX1/2_LOCK = '1' indicates that the Receiver PLL is locked. If RX1/2_LOCK is de-asserted, the Receiver is not ready.

RX1/2_EQSEL activates the internal equalizer to support extended cable lengths over 10 meters.

The status bit RX1/2_LSYNC# is asserted if the GigaSTaR Receiver has successfully synchronized to the incoming bit-stream. If the Receiver is not synchronized correctly, RX1/2_LSYNC# is de-asserted.

RX1/2_PERR# : the receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of both parity information indicates a transmission failure and the signal RX1/2_PERR# is asserted for one data cycle. RX1/2_LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

The RX1/2_FLAGO output provides the internal flag controlled by the TX1/2_FLAGI input. After a reset, the status of RX1/2_FLAGO is "low".

1.6 LINK MEDIA

The GigaSTaR Transmitter and Receiver are each equipped with a robust high-speed interface which can be directly connected to impedance-controlled cables (STP or coax), transmission lines or fiber optic modules.

The ING_TTC/RRC Piggyback Boards are configured to drive a 50 Ohm (100 Ohm differential) Shielded-Twisted-Pair (STP) cable with a SUB D9 connector. Initial evaluations with 50 Ohm (100 Ohm differential) Shielded-Twisted-Pair (STP) cables already have proven reliable transmissions at distances of up to 50 meters and beyond. The reference cables GGSC1608-05/-10/-15/-20/-30/-40/-50 by W.L. Gore & Associates contain 2 twisted pairs of wires, allowing a dual link configuration as shown in Fig. 3:

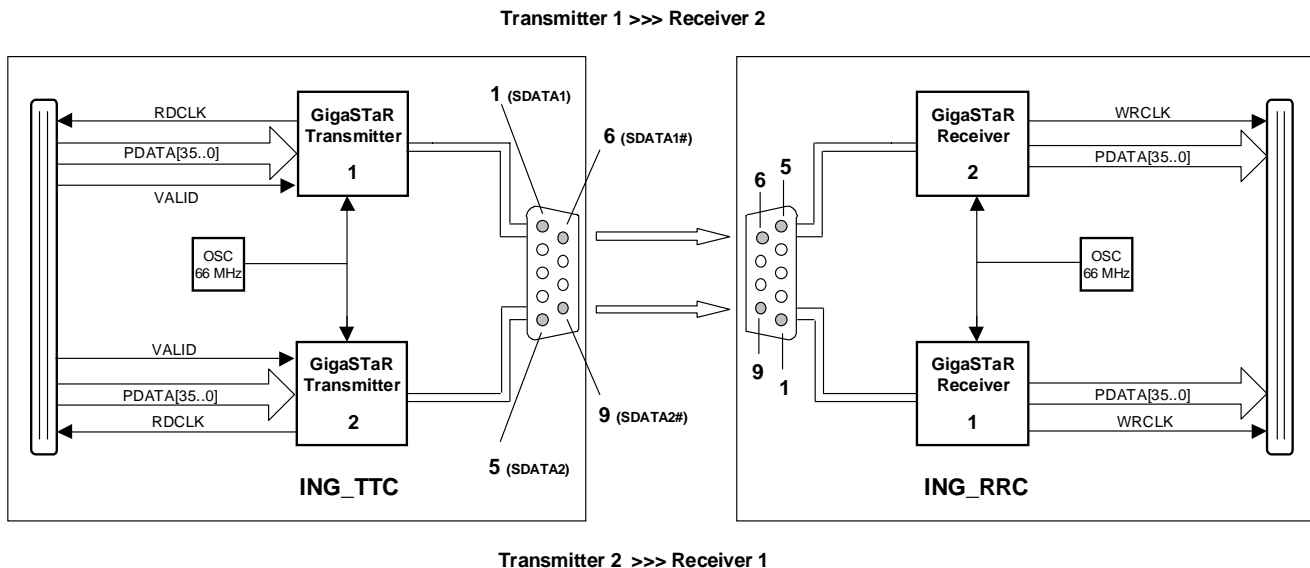


Figure 3: Transmission schemes ING_TTC to ING_RRC boards using GORE GGSC1608-x cable

Please note that through the configuration of the GORE GGSC1608-x cable, the transmitter device #1 will be connected to receiver device #2 and the transmitter device #2 will be connected to receiver device #1.

1.7 TRANSMITTER SIGNAL TIMINGS (ING_TTC)

1.7.1 Data Burst Transfers

The data burst timing provides the full data rate of 148.5 MByte/s per link. TX1/2_VALID is asserted when the first data is valid at TX1/2_PD [35..0]. With every rising edge of TX1/2_RDCLK the TX1/2_PD inputs are registered, serialized and transmitted. TX1/2_VALID can remain asserted as long as new data are available.

In the timing diagram TX1/2_PARGEN is de-asserted and the application delivers the TX1/2_PARITY bit synchronously to the data word.

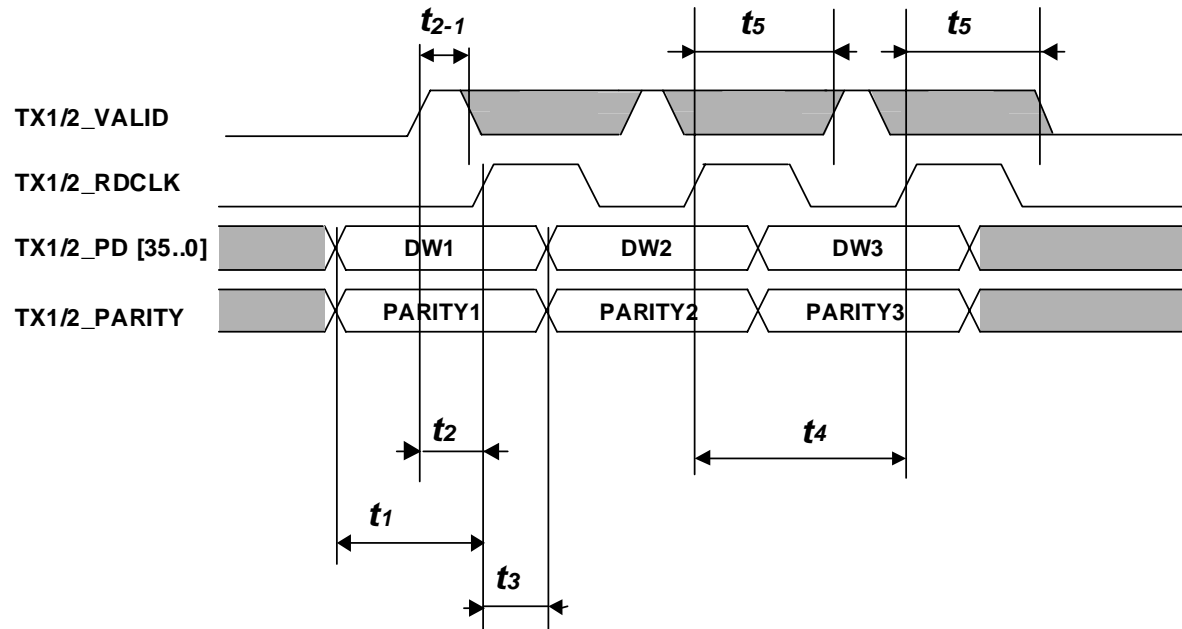


Figure 4: Transmitter Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t ₁	Setup time TX1/2_PD and TX1/2_PARITY to TX1/2_RDCLK rising edge	9	6		ns
t ₂	TX1/2_VALID active to first rising TX1/2_RDCLK edge	9	12	14	ns
t ₂₋₁	TX1/2_VALID high state	5	4		ns
t ₃	TX1/2_PD and TX1/2_PARITY hold time	9	6		ns
t ₄	TX1/2_RDCLK cycle time (without assertion of TX1/2_FLAGI)		30.3		ns
t ₅	Rising TX1/2_RDCLK edge to sampling window for TX1/2_VALID state (TX1/2_VALID=0 : exit BURST mode, TX1/2_VALID=1: continue BURST mode)	18	20	22	ns

Note: For timings with assertion of FLAGI, please see section 1.9

Table 1: Transmitter Data Burst Timing Parameters (under recommended operating conditions)

1.7.2 Single Word Transfers

Single Word Transfers are used to support lower data rates than the maximum parallel data rate per link of 148.5 MByte/s. TX1/2_VALID has to be de-asserted after the parallel read cycle signalled by one TX1/2_RDCLK pulse. Only one data word is transmitted.

In the timing diagram TX1/2_PARGEN is de-asserted and the application delivers the TX1/2_PARITY bit synchronously to the data word.

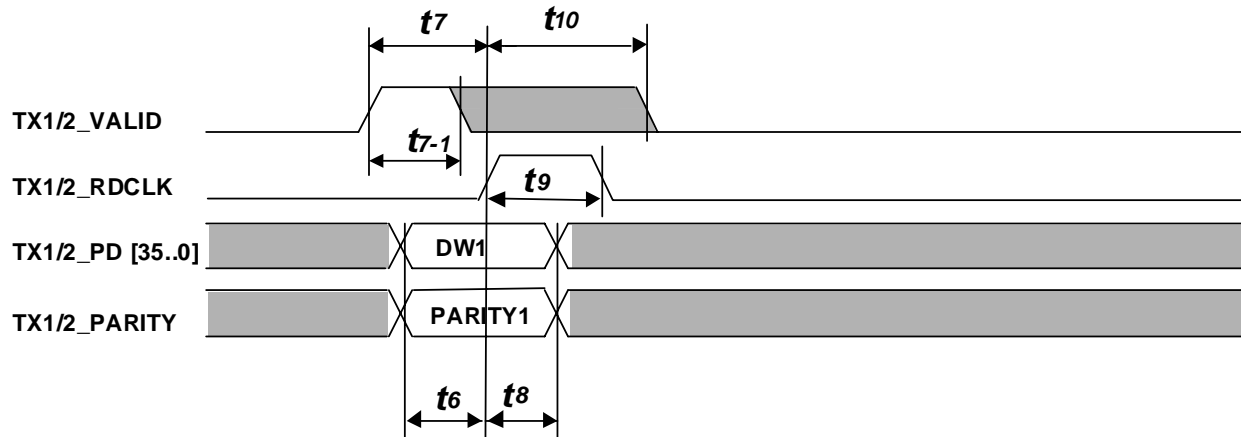


Figure 5: Receiver Single Word Transfer Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t ₆	Setup time TX1/2_PD and TX1/2_PARITY to TX1/2_RDCLK rising edge	9	6		ns
t ₇	TX1/2_VALID active to rising TX1/2_RDCLK edge	9	12	14	ns
t ₇₋₁	TX1/2_VALID high state	5	4		ns
t ₈	TX1/2_PD and TX1/2_PARITY hold time	9	6		ns
t ₉	TX1/2_RDCLK high state (without assertion of TX1/2_FLAGI)	14	15	16	ns
t ₁₀	Rising TX1/2_RDCLK edge to sampling window for TX1/2_VALID state (TX1/2_VALID=0: continue single word mode, TX1/2_VALID=1: enter BURST mode)	18	20	22	ns

Note : For timings with assertion of FLAGI, please see section 1.9

Table 2: Receiver Single Word Transfer Timing Parameters (under recommended operating conditions)

1.8 RECEIVER SIGNAL TIMINGS (ING_RRC)

1.8.1 Data Burst Transfers

The data burst timing is used to support the full data rate of 148.5 MByte/s per link. RX1/2_PD [35..0] and RX1/2_PARITY are updated with each rising edge of RX1/2_WRCLK (see figure 6).

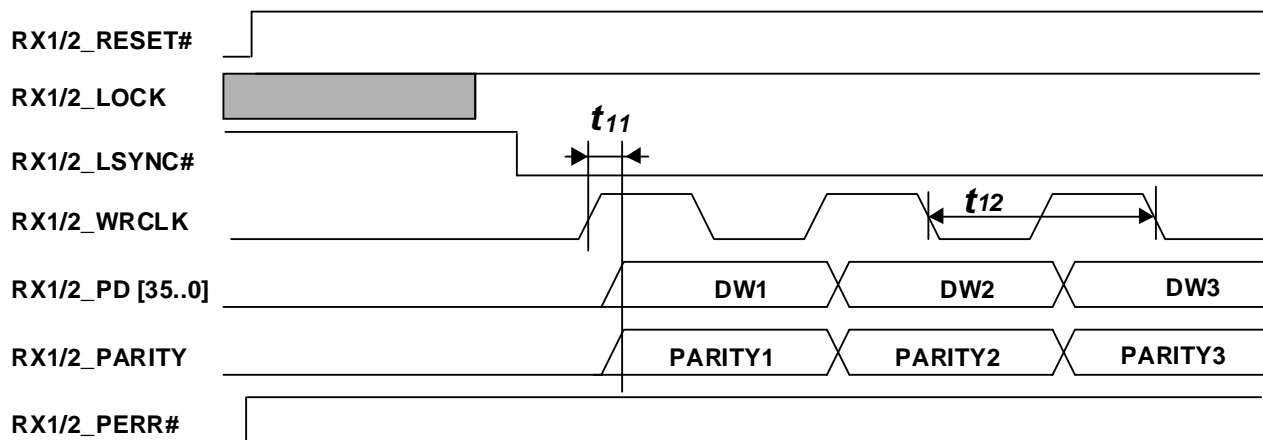


Figure 6: Receiver Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_{11}	Rising edge RX1/2_WRCLK to RX1/2_PD and RX1/2_PARITY bit valid		1	4	ns
t_{12}	RX1/2_WRCLK cycle time (without assertion of TX1/2_FLAGI)		30.3		ns

Note: For timings with assertion of TX1/2_FLAGI, please see section 1.9

Table 3: Receiver Data Burst Timing Parameters (under recommended operating conditions)

1.8.2 Single Word Transfers

Single Word Transfers are used to support lower data rates. Every time a new data word is received the RX1/2_WRCLK signal generates one clock pulse.

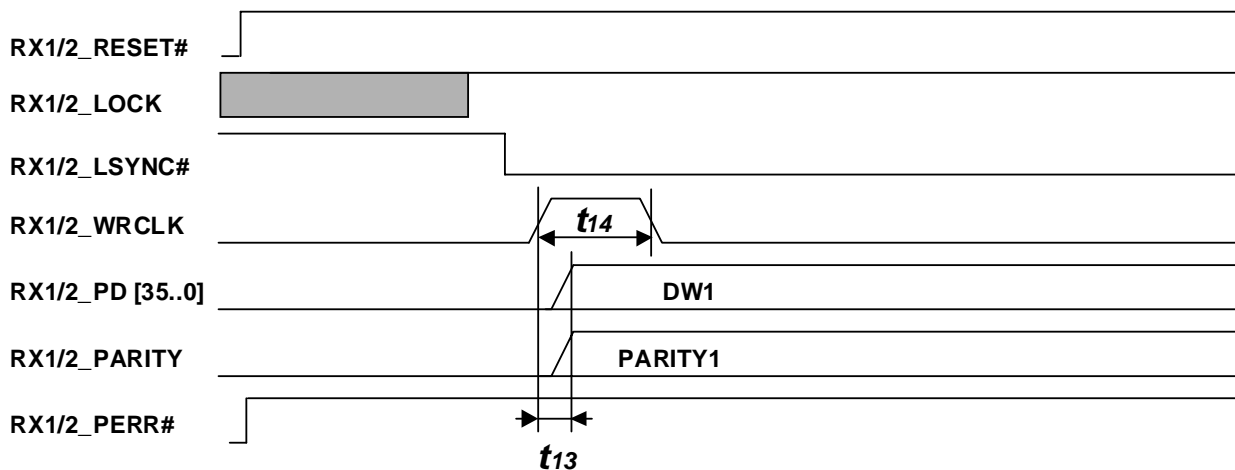


Figure 7: Receiver Single Word Transfer Timing Diagram

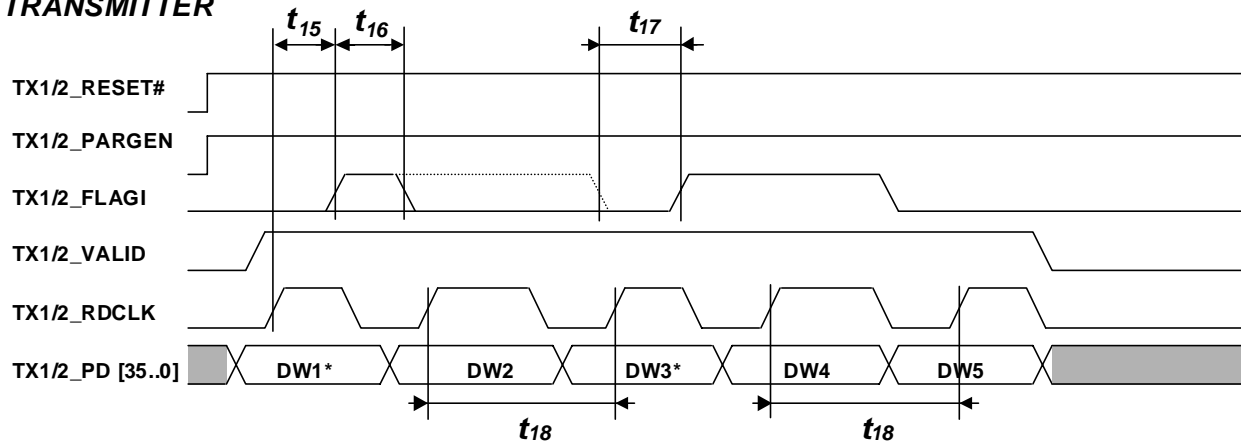
Parameter	Description	Min.	Typ.	Max.	Unit
t ₁₃	Rising edge RX1/2_WRCLK to RX1/2_PD and RX1/2_PARITY valid		1	4	ns
t ₁₄	RX1/2_WRCLK high state	14	15	16	ns

Table 4: Receiver Single Word Transfer Timing Parameters (under recommended operating conditions)

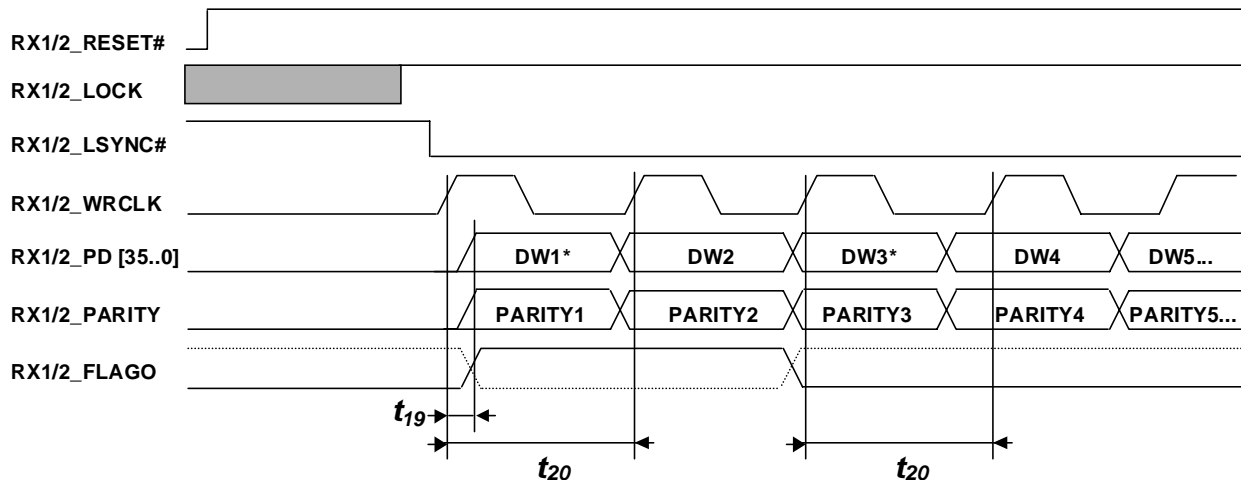
1.9 TRANSMITTER FLAGI SIGNAL TIMING / RECEIVER FLAGO SIGNAL TIMING

With the TX1/2_FLAGI / RX1/2_FLAGO signals a mechanism is provided to implement a side band signalling. Each rising edge at the Transmitter's input TX1/2_FLAGI toggles the RX1/2_FLAGO output of the Receiver. The timing diagram for the TX1/2_FLAGI/RX1/2_FLAGO signal is shown in combination with the Transmitter signals. Note that when the TX1/2_FLAGI signal is asserted, the following TX1/2_RDCLK high state time span is enlarged by app. 6 ns. At the Receiver, the RX1/2_WRCLK low state time span is enlarged by app. 6 ns when the RX1/2_FLAGO output toggles. In the diagrams below, the TX1/2_PARGEN is active at the Transmitter therefore no external parity is provided.

TRANSMITTER



RECEIVER



Note : * indicates the data words [DW1, DW3] that are marked by the TX1/2_FLAGI signal.

Figure 8: INGT165B / INGR165B TX1/2_FLAGI and RX1/2_FLAGO Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t ₁₅	Rising edge of TX1/2_RDCLK to rising edge of TX1/2_FLAGI	0		18	ns
t ₁₆	TX1/2_FLAGI minimum high state		4	6	ns
t ₁₇	TX1/2_FLAGI minimum low state		4	6	ns
t ₁₈	TX1/2_RDCLK cycle time after assertion of TX1/2_FLAGI (one cycle only)		36		ns
t ₁₉	Rising edge of RX1/2_WRCLK to RX1/2_PD, RX1/2_PARITY and RX1/2_FLAGO valid		1	4	ns
t ₂₀	RX1/2_WRCLK cycle time for data word marked by RX1/2_FLAGO toggle		36		ns

Table 5: TX1/2_FLAGI and RX1/2_FLAGO Timing Parameters (under recommended operating conditions)

1.10 ERROR (REPORTING) TIMING (ING_RRC)

1.10.1 Parity Error (Reporting) Timing

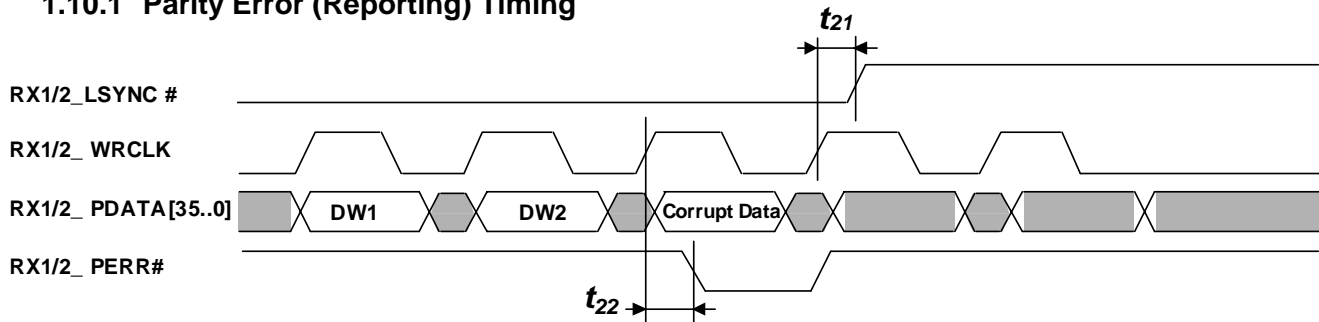


Figure 9: Parity Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
t ₂₁	Rising edge of RX1/2_WRCLK after the corrupt data word to rising edge of RX1/2_LSYNC#		1	5	ns
t ₂₂	Rising edge of RX1/2_WRCLK marking the corrupt data word to falling edge of RX1/2_PERR#		3	6	ns

Table 6: Parity Error (reporting) timing (under recommended operating conditions)

1.10.2 Header/Frame Error (reporting) timing

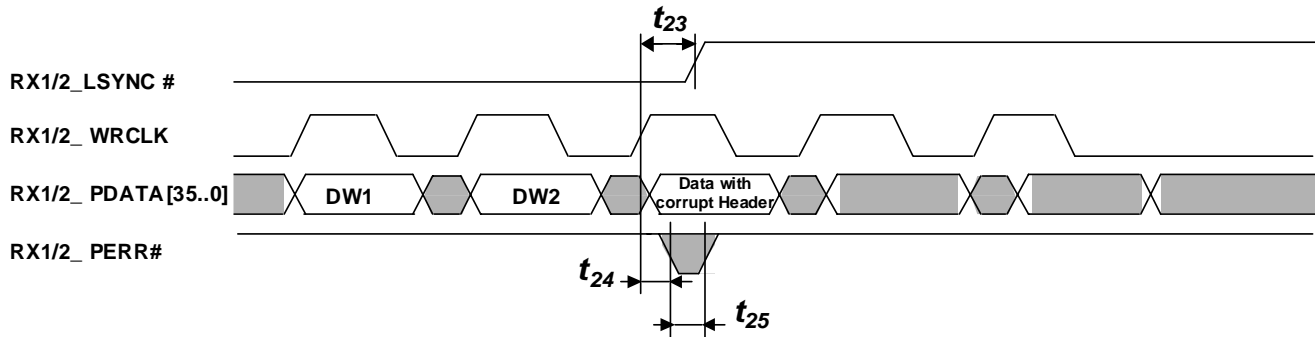


Figure 10: Header/Frame Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{23}	Rising edge of RX1/2_WRCLK marking the corrupt data header to rising edge of RX1/2_LSYNC#	0		13	ns
t_{24}	Rising edge of RX1/2_WRCLK marking the corrupt data header to falling edge of RX1/2_PERR#		1,5		ns
t_{25}	RX1/2_PERR # low state		3		ns

Table 7: Header/Frame Error (reporting) timing (under recommended operating conditions)

2. PIGGYBACK BOARD INTERFACE AND MOUNTING DESCRIPTION

2.1 ING_TTC PIGGYBACK AMP 140 PIN CONNECTOR DEFINITION

Pin	Signal	Pin	Signal	Pin	Signal
4	TX1_PD0	82	TX2_PD0	2	GND
6	TX1_PD1	84	TX2_PD1	11	GND
8	TX1_PD2	86	TX2_PD2	22	GND
10	TX1_PD3	88	TX2_PD3	31	GND
14	TX1_PD4	92	TX2_PD4	42	GND
16	TX1_PD5	94	TX2_PD5	51	GND
18	TX1_PD6	96	TX2_PD6	61	GND
20	TX1_PD7	98	TX2_PD7	65	GND
13	TX1_PD8	93	TX2_PD8	69	GND
15	TX1_PD9	95	TX2_PD9	73	GND
17	TX1_PD10	97	TX2_PD10	79	GND
25	TX1_PD11	103	TX2_PD11	90	GND
19	TX1_PD12	101	TX2_PD12	99	GND
24	TX1_PD13	102	TX2_PD13	110	GND
26	TX1_PD14	104	TX2_PD14	119	GND
28	TX1_PD15	106	TX2_PD15	130	GND
30	TX1_PD16	108	TX2_PD16	139	GND
27	TX1_PD17	105	TX2_PD17	1	VCC
29	TX1_PD18	107	TX2_PD18	12	VCC
34	TX1_PD19	112	TX2_PD19	21	VCC
33	TX1_PD20	111	TX2_PD20	32	VCC
36	TX1_PD21	114	TX2_PD21	41	VCC
37	TX1_PD22	115	TX2_PD22	52	VCC
38	TX1_PD23	116	TX2_PD23	62	VCC
35	TX1_PD24	113	TX2_PD24	80	VCC
39	TX1_PD25	117	TX2_PD25	89	VCC
40	TX1_PD26	118	TX2_PD26	100	VCC
44	TX1_PD27	122	TX2_PD27	109	VCC
45	TX1_PD28	123	TX2_PD28	120	VCC
54	TX1_PD29	132	TX2_PD29	129	VCC
48	TX1_PD30	126	TX2_PD30	140	VCC
53	TX1_PD31	131	TX2_PD31	23, 91	Reserved, set to GND (*)
47	TX1_PD32	125	TX2_PD32	63	Reserved, set to VCC (*)
56	TX1_PD33	134	TX2_PD33	67, 71	Reserved, do not connect (*)
49	TX1_PD34	127	TX2_PD34	57, 59, 60	Not connected
55	TX1_PD35	133	TX2_PD35	64, 66, 68	Not connected
7	TX1_LOCK	85	TX2_LOCK	70, 72, 74	Not connected
9	TX1_PARITY	87	TX2_PARITY	75, 76, 77	Not connected
58	TX1_PERR#	136	TX2_PERR#	78, 135	Not connected
3	TX1_RESET#	81	TX2_RESET#	137, 138	Not connected
5	TX1_RDCLK	83	TX2_RDCLK		
43	TX1_FLAGI	121	TX2_FLAGI		
46	TX1_PARGEN	124	TX2_PARGEN		
50	TX1_VALID	128	TX2_VALID		(*) : These pins are reserved for optional functions

Table 8: Piggyback AMP 140 Pin Free Height Connector Pin Definition (AMP #179029-6)

Note: By choosing an AMP free height receptacle AMP part # AMP177983-6/AMP5-179009-6/AMP 5-179010-6, the spacing between the piggyback board and the main board can be selected to be 6, 10 or 14 mm.

2.2 ING_RRC PIGGYBACK AMP 140 PIN CONNECTOR DEFINITION

Pin	Signal	Pin	Signal	Pin	Signal
82	RX1_PD0	4	RX2_PD0	2	GND
84	RX1_PD1	6	RX2_PD1	11	GND
86	RX1_PD2	8	RX2_PD2	22	GND
88	RX1_PD3	10	RX2_PD3	31	GND
92	RX1_PD4	14	RX2_PD4	42	GND
94	RX1_PD5	16	RX2_PD5	51	GND
96	RX1_PD6	18	RX2_PD6	61	GND
98	RX1_PD7	20	RX2_PD7	65	GND
93	RX1_PD8	13	RX2_PD8	69	GND
95	RX1_PD9	15	RX2_PD9	73	GND
97	RX1_PD10	17	RX2_PD10	79	GND
103	RX1_PD11	25	RX2_PD11	90	GND
101	RX1_PD12	19	RX2_PD12	99	GND
102	RX1_PD13	24	RX2_PD13	110	GND
104	RX1_PD14	26	RX2_PD14	119	GND
106	RX1_PD15	28	RX2_PD15	130	GND
108	RX1_PD16	30	RX2_PD16	139	GND
105	RX1_PD17	27	RX2_PD17	1	VCC
107	RX1_PD18	29	RX2_PD18	12	VCC
112	RX1_PD19	34	RX2_PD19	21	VCC
111	RX1_PD20	33	RX2_PD20	32	VCC
114	RX1_PD21	36	RX2_PD21	41	VCC
115	RX1_PD22	37	RX2_PD22	52	VCC
116	RX1_PD23	38	RX2_PD23	62	VCC
113	RX1_PD24	35	RX2_PD24	80	VCC
117	RX1_PD25	39	RX2_PD25	89	VCC
118	RX1_PD26	40	RX2_PD26	100	VCC
122	RX1_PD27	44	RX2_PD27	109	VCC
123	RX1_PD28	45	RX2_PD28	120	VCC
132	RX1_PD29	54	RX2_PD29	129	VCC
126	RX1_PD30	48	RX2_PD30	140	VCC
131	RX1_PD31	53	RX2_PD31		
125	RX1_PD32	47	RX2_PD32	63	Reserved, set to VCC (*)
134	RX1_PD33	56	RX2_PD33	67, 71	Reserved, do not connect (*)
127	RX1_PD34	49	RX2_PD34	46, 124	Not connected
133	RX1_PD35	55	RX2_PD35	57, 59, 60	Not connected
87	RX1_LOCK	7	RX2_LOCK	64, 66, 68	Not connected
91	RX1_PARITY	9	RX2_PARITY	70, 72, 74	Not connected
136	RX1_PERR#	58	RX2_PERR#	75, 76, 77	Not connected
81	RX1_RESET#	3	RX2_RESET#	78, 135	Not connected
83	RX1_WRCLK	5	RX2_WRCLK	137, 138	Not connected
121	RX1_FLAGO	43	RX2_FLAGO		
128	RX1_LSYNC#	50	RX2_LSYNC#		
85	RX1_EQSEL	23	RX2_EQSEL		(*) : These pins are reserved for optional functions

Table 9: Piggyback AMP 140 Pin Free Height Connector Pin Definition (AMP #179029-6)

Note: By choosing an AMP free height receptacle AMP part # AMP177983-6/AMP5-179009-6/AMP 5-179010-6, the spacing between the piggyback board and the main board can be selected to be 6, 10 or 14 mm.

The pin numbering definition of the AMP connector is shown in Fig. 11:

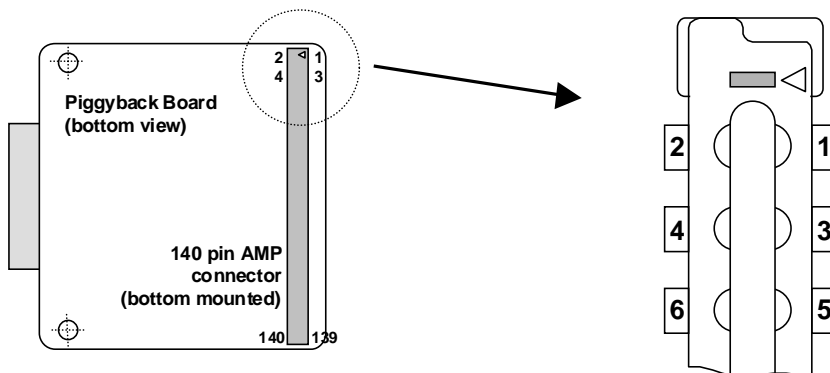


Fig. 11: Piggyback AMP 140 pin free height connector numbering

2.3 SERIAL TRANSMISSION CABLE TERMINATION (ING_RRC)

The SUB D9 cable connector plugs directly into the transmission reference cables (GGSC1608-05/-10/-15/-20/-25/-30, W.L. Gore & Associates). Besides the AC coupling capacitors providing 50 V DC isolation per line end, a dedicated cable termination is mounted on the bottom side of the piggyback board to the SUB D9 connector pins. The default delivery termination is matched for the GGSC1608-10 (10 meter Gore GigaSTaR cable). As the inductance value of this termination is a function of the transmission cable characteristic, the termination has to be matched to the cable if another cable than GGSC1608-10 is used:

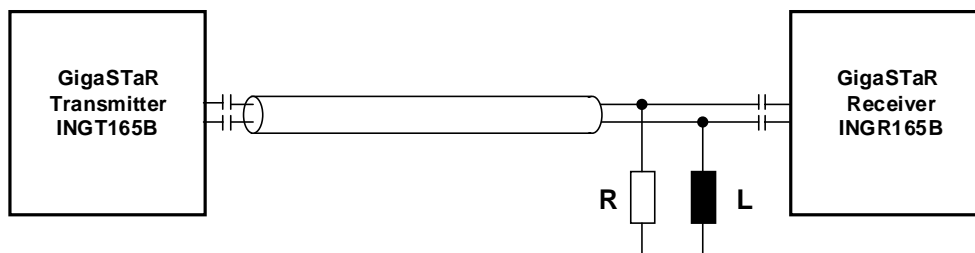


Figure 12: Piggyback serial transmission cable termination scheme

Gore cable type number	Cable length	R value (SMD type 0805)	L value (SMD type 1210)
GGSC1608-05	5 meter	100 Ohm	22 nH
GGSC1608-10 (delivery configuration)	10 meter	100 Ohm	47 nH
GGSC1608-20	20 meter	100 Ohm	220 nH
GGSC1608-30	30 meter	150 Ohm	220 nH

Table 10: Various Gore GGSC1608 cable lengths with corresponding termination values

Note : For other cable lengths or cable types than shown in table 10, other termination values may apply, please call your distributor support line for further information.

The termination devices are mounted on the bottom side of the ING_RRC board SUB D9 connector, on the solder flags as shown in Figure 13:

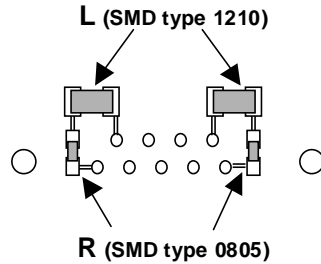


Figure 13: ING_RRC piggyback board serial transmission cable termination components

3. PIGGYBACK BOARD SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	-0.5	+4.2	V	
Input Voltage	V_{IN}	-0.5	$V_{CC}+0.5$	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	
Ambient Temperature (under bias)	T_B	-40	+70	° C	
Storage Temperature	T_{stg}	-40	+85	° C	
Static Discharge Voltage (AMP connector pins)	V_{SDAMP}		± 2000	V	Human Body Model
Static Discharge Voltage (DB9 connector pins)	V_{SDDb9}		± 800	V	Human Body Model

Table 11: Absolute Maximum Ratings

3.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	+3.15	+3.45	V	
Input Voltage	V_{IN}	0	V_{CC}	V	$V_{CC} = 3.3V \pm 0.15V$
Ambient Temperature	T_a	-40	+70	° C	Air flow ≥ 250 LFPM

Table 12: Recommended Operating Conditions

3.3 ELECTRICAL SPECIFICATION

3.3.1 DC – Characteristics (under recommended operating conditions)

Parameter	Symb ol	Test Condition	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}		2.6			V
Input Low Voltage	V_{IL}				0.7	V
Input High Current	I_{IH}	$V_{IN} = V_{CC}$	-10		10	μA
Input Low Current	I_{IL}	$V_{IN} = 0 V$	-10		-150	μA
Output High Voltage	V_{OH}	$I_{OH} = -0.5 mA$	0,95 V_{CC}			V
Output Low Voltage	V_{OL}	$I_{OL} = 1.5 mA$			0,05 V_{CC}	V
LOCK Output High Current	V_{LH}	$I_{OH} = -0.5 mA$	0,9 V_{CC}			mA
LOCK Output Low Current	V_{LL}	$I_{OL} = 1.5 mA$			0,1 V_{CC}	mA
Supply Current	I_{CC}	Max. data transmission rate		600	850	mA
Power Dissipation	P_D	Max. data transmission rate		2,0	2,9	W

Table 13: DC – Characteristics

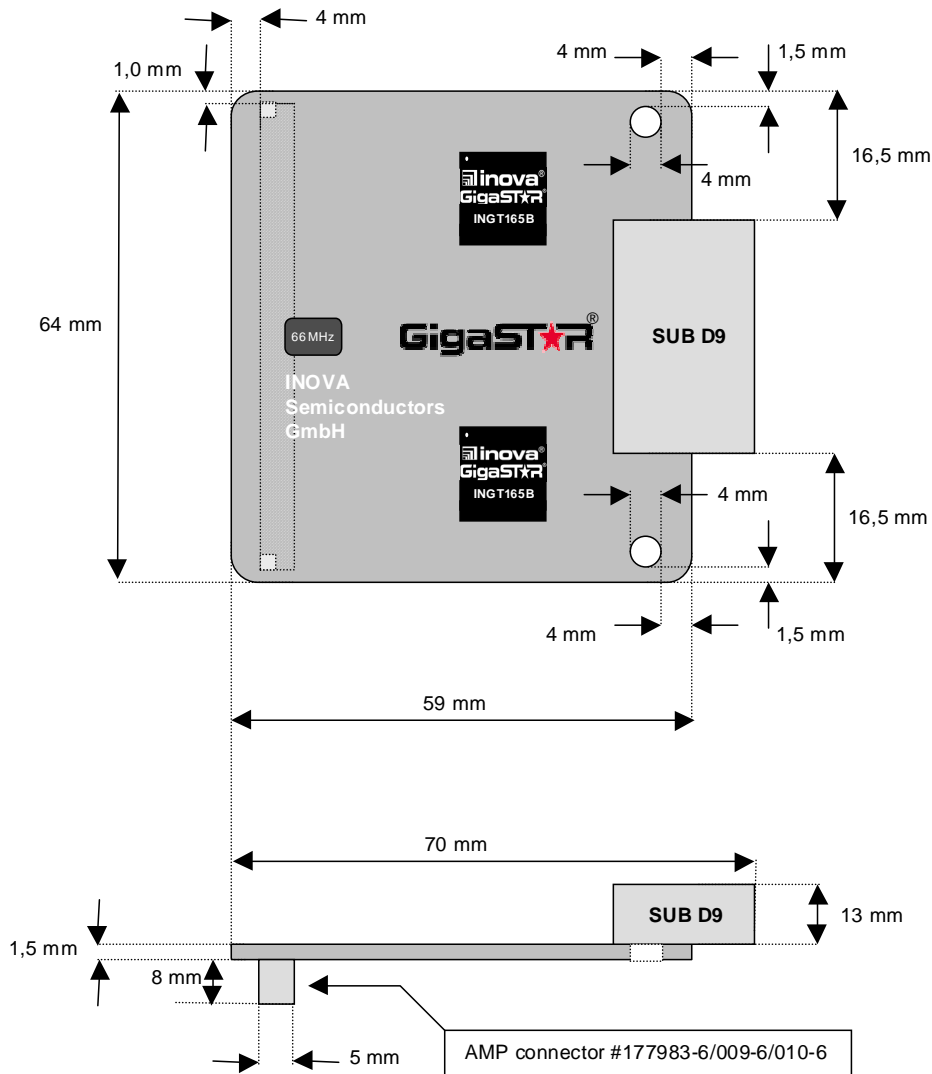
3.3.2 AC- Characteristics (under recommended operating conditions)

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Setup time TX1/2_PD and TX1/2_PARITY to TX1/2_RDCLK rising edge	9	6		ns
t_2	TX1/2_VALID active to first rising TX1/2_RDCLK edge	9	12	14	ns
t_{2-1}	TX1/2_VALID high state	5	4		ns
t_3	TX1/2_PD and TX1/2_PARITY hold time	9	6		ns
t_4	TX1/2_RDCLK cycle time (without assertion of TX1/2_FLAGI)		30.3		ns
t_5	Rising TX1/2_RDCLK edge to sampling window for TX1/2_VALID state (TX1/2_VALID=0 : exit BURST mode, TX1/2_VALID=1: continue BURST mode)	18	20	22	ns
t_6	Setup time TX1/2_PD and TX1/2_PARITY to TX1/2_RDCLK rising edge	9	6		ns
t_7	TX1/2_VALID active to rising TX1/2_RDCLK edge	9	12	14	ns
t_{7-1}	TX1/2_VALID high state	5	4		ns
t_8	TX1/2_PD and TX1/2_PARITY hold time	9	6		ns
t_9	TX1/2_RDCLK high state (without assertion of TX1/2_FLAGI)	14	15	16	ns
t_{10}	Rising TX1/2_RDCLK edge to sampling window for TX1/2_VALID state (TX1/2_VALID=0: continue single word mode, TX1/2_VALID=1: enter BURST mode)	18	20	22	ns
t_{11}	Rising edge RX1/2_WRCLK to RX1/2_PD and RX1/2_PARITY bit valid		1	4	ns
t_{12}	RX1/2_WRCLK cycle time (without assertion of TX1/2_FLAGI)		30.3		ns
t_{13}	Rising edge RX1/2_WRCLK to RX1/2_PD and RX1/2_PARITY valid		1	4	ns
t_{14}	RX1/2_WRCLK high state	14	15	16	ns
t_{15}	Rising edge of TX1/2_RDCLK to rising edge of TX1/2_FLAGI	0		18	ns
t_{16}	TX1/2_FLAGI minimum high state		4	6	ns
t_{17}	TX1/2_FLAGI minimum low state		4	6	ns
t_{18}	TX1/2_RDCLK cycle time after assertion of TX1/2_FLAGI (one cycle only)		36		ns
t_{19}	Rising edge of RX1/2_WRCLK to RX1/2_PD, RX1/2_PARITY and RX1/2_FLAGO valid		1	4	ns
t_{20}	RX1/2_WRCLK cycle time for data word marked by RX1/2_FLAGO toggle		36		ns

t ₂₁	Rising edge of RX1/2_WRCLK after the corrupt data word to rising edge of RX1/2_LSYNC#		1	5	ns
t ₂₂	Rising edge of RX1/2_WRCLK marking the corrupt data word to falling edge of RX1/2_PERR#		3	6	ns
t ₂₃	Rising edge of RX1/2_WRCLK marking the corrupt data header to rising edge of RX1/2_LSYNC#	0		13	ns
t ₂₄	Rising edge of RX1/2_WRCLK marking the corrupt data header to falling edge of RX1/2_PERR#		1,5		ns
t ₂₅	RX1/2_PERR # low state		3		ns

Table 14: Transmitter and Receiver Timing Parameters (under recommended operating conditions)

3.4 PIGGYBACK BOARD DIMENSIONS (identical for ING_TTC & ING_RRC boards)



All dimensions are given in millimeters

Figure 14: Top and side view of the Piggyback Board with mechanical outlines

3.5 HANDLING PRECAUTIONS

Handling precautions are:

1. The maximum ratings may not be exceeded at any time.
2. Precautions have to be taken against exposure of the board terminals to electrostatic discharge stress.
3. Mounting and dismounting of the AMP connector and receptacles have to be performed with care.
4. The mounting/dismounting cycles should be limited in order to avoid AMP connector wearout.
5. For ambient temperatures exceeding 50°C, an air flow of ≥ 250 LFPM should be provided.
6. The piggyback board is not EME-shielded and must not be operated in an environment where its electromagnetic emissions can cause malfunctions of other boards or devices.

3.6 ORDERING CODE AND PRODUCTION STATUS INFORMATION

Ordering Code	Delivery option	Production Status
ING_TTC	Piggyback double Transmitter Board configured for the 10 m Gore GGSC1608-10 cable	Released to full production
ING_RRC	Piggyback double Receiver Board configured for the 10 m Gore GGSC1608-10 cable	Released to full production

Table 15: Product Availability

Inova Semiconductors GmbH

Ismaninger Str. 3
D-81675 Munich, Germany
Phone: +49 (0)89 / 45 74 75 - 60
Fax: +49 (0)89 / 45 74 75 - 88
Email: info@inova-semiconductors.de
URL: <http://www.inova-semiconductors.com>

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