



TD1120

USB On-The-Go Full Speed Host and High Speed Peripheral Controller

Description

TransDimension's TD1120 is a single chip Full Speed USB Host and High Speed USB Peripheral controller that is the third controller in the family of integrated low-cost, high-performance, On-the-Go (OTG) controllers optimized and specifically designed for embedded systems, peripherals, mobile communication, and consumer products. The TD1120 is a combination of a standard full speed USB host controller and a high speed peripheral controller. The TD1120 enables embedded systems to operate as a USB Host and a Peripheral, thereby dramatically expanding the degree of interconnectivity and extending the applicability of USB into many new areas, especially low power, mobile markets. It allows high-speed transfers at 480Mb/s when connected to a host, but down shifts to a full speed host at 12Mb/s when in a mobile environment where lower power is essential. Software solutions for the TD1120 is available from SoftConnex Technologies, Inc., a wholly owned subsidiary of TransDimension Inc., which includes USBLink OTG Stack, ported to a wide variety of RTOSs, interface code to the TD1120 and USB device drivers. Peer-to-Peer connectivity is made simple with the TD1120 since USB connectivity is achieved without PC intervention. Applications include mobile and post-PC products such as cellular phones, palmtop PCs, PDAs, MP3 players, projectors, and Internet appliances, to name a few. The TD1120 is very flexible and can operate in several modes, including

- USB On-the-Go dual-role device: One OTG port plus a standard host with one downstream port
- Simultaneous high-speed USB Peripheral controller and two standard hosts with two downstream ports

The host controller in the TD1120 is the same as the TD242LP and is the only true transfer level embedded USB host and On-the-Go controller that can be interfaced directly to most popular microprocessors and is easily programmable. The active endpoint and transfer descriptors are located in the on-chip memory, thus significantly reducing processor overhead relative to any comparable product on the market.

The high-speed Peripheral controller is very flexible and software configurable, in terms of the active bi-directional endpoint number (8), type, size, and buffering mechanism of each endpoint.

Features

- High-performance, Full Speed USB host and High Speed Peripheral controller
- Low CPU utilization
- Fully compliant with USB Specification Rev. 2.0 and USB On-the-Go specifications.
- Configurable software and hardware Host Negotiation Protocol and Session Request Protocol
- Transaction scheduling and transfer level protocol implemented in hardware including bandwidth management, data toggle and retry
- Isochronous transfers with loose timing requirements on the microprocessor
- Fast microprocessor access cycle and double/multi buffering support for all four types of USB transfers
- Power saving mode for whole chip and host controller, and suspend mode for peripheral controller
- Integrated PLL supports external crystal or crystal oscillators of 12MHz and 30MHz
- Single 3.3V power supply, flexible I/O voltage of 2.5V to 3.3 V (LVCMOS/TTL)
- Built-in voltage regulator from external 3.3V to 2.5V
- Integrated on-chip charge pump, supports up to 50mA of current
- Maximum current of <40mA for Host operation and <80mA for Peripheral operation
- Small packages of 84-ball 7x7mm TF-BGA & 100-pin 12x12mm LQFP packages
- Direct interface to microprocessors, RISC, CISC, and DSPs including but not limited to x86, Intel XScale & StrongARM, Hitachi SH3, Fujitsu SPARCLite, NEC and Toshiba MIPS, ARM7, ARM9, Motorola PowerPC, ColdFire and Dragonball among others
- Embedded RTOS software available for WinCE, Linux, VxWorks, Nucleus, LynxOS, QNX, pSOS, PowerTV, SMX, AMX, ThreadX, VRTX, ITRON, Symbian OS and MS-DOS operating systems among others
- USB device driver software available including printer, speaker, mass storage, hub, modem, Ethernet, mouse, keyboard, digital camera, video camera, cell phone, STB, PDA, etc.
- Two DMA (slave) channels for Peripheral
- 8K bytes of on-chip RAM

Architecture

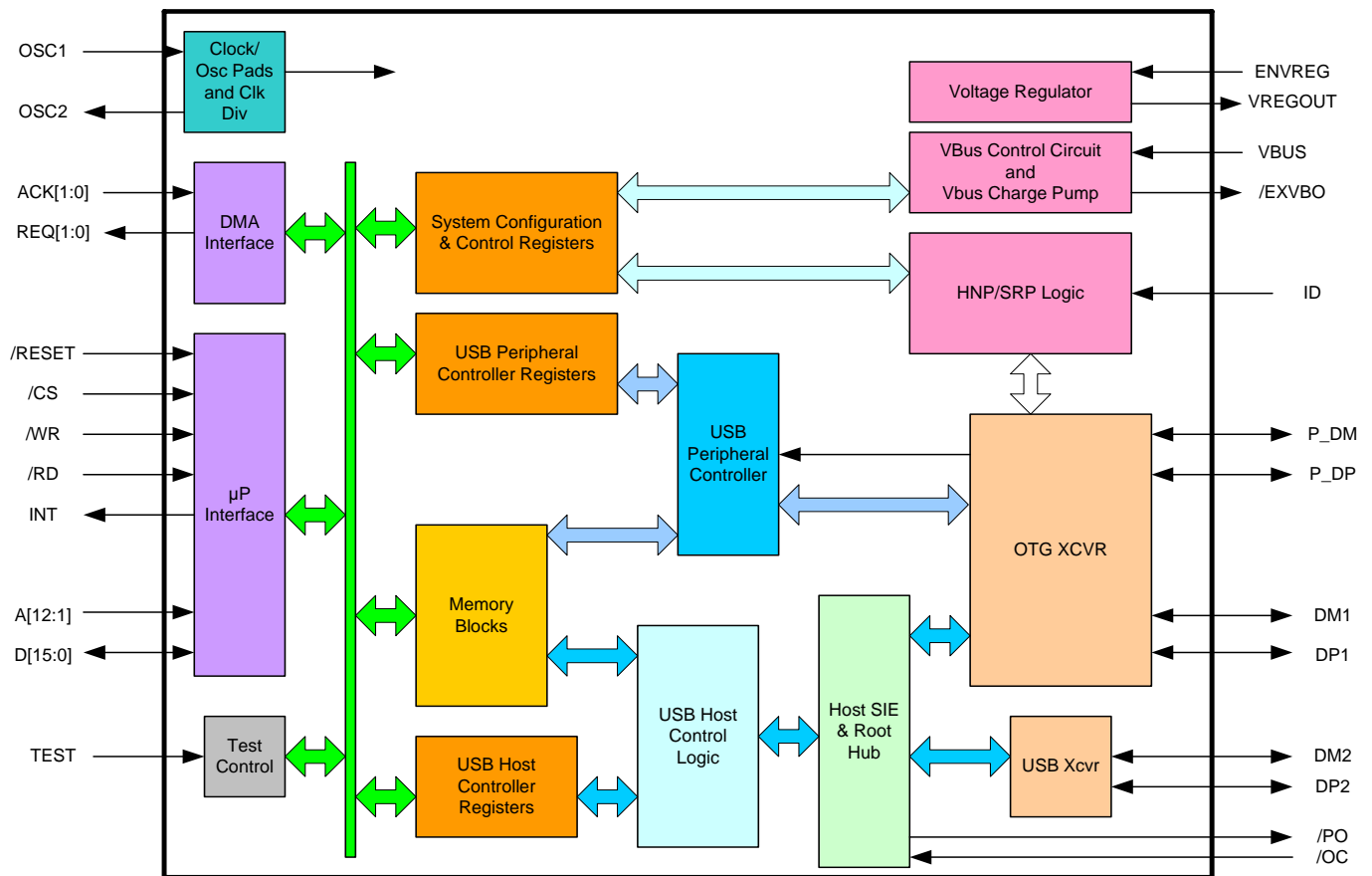


Figure 1 – TD1120 Architectural Block Diagram

USB/OTG Host logic blocks: The USB Host Controller Logic, the Host Serial Interface Engine (SIE) and the root hub are responsible for the fully compliant (not reduced) USB Host of the TD1120 - supporting transfer level user interface, scheduling/processing transactions, and monitoring/handling port events.

USB/OTG Peripheral logic blocks: The High Speed USB Peripheral Controller Logic, together with the Peripheral SIE, manages all low-level USB peripheral protocols upon which a fully compliant high speed USB peripheral is operated.

Interrupt Handling: Interrupts from the TD1120 to a microprocessor are minimum, as an interrupt is generated only at the end of a USB transfer (for both Host and Peripheral), which can have a size of up to 4 Mbytes. Moreover, an interrupt event may be delayed inside the TD1120, and be bundled with others to further reduce the number of interrupt occurrences.

Memory blocks: The Host Controller Logic, the Peripheral Controller logic, and the microprocessor are all entitled to have access to the memory blocks for data and control. A RAM Arbiter sequences all RAM access.

Register banks: There are 3 register banks used for System Configuration, Host Control, and Peripheral Control.

Host Negotiation Protocol (HNP): Hardware HNP is a built-in state machine, which reduces microprocessor interrupts. HNP, when enabled, will support negotiation with an attached OTG device, in order to determine which role, (A-device or B-device) the TD1120 will operate within a session. The TD1120 contains the required analog components (comparators, etc.) and digital logic to support the operation. The microprocessor interfaced to the TD1120 can also disable this HNP and configure the dual-role device port of the TD1120 to operate as a Host or Peripheral. HNP may only be implemented in conjunction with a Mini-AB receptacle.

Session Request Protocol (SRP): The USB OTG specification is positioned to service mobile products that are battery powered. The SRP protocol allows the A-device to conserve power by turning the USB VBus signal off depending on whether there is USB traffic, whereas, in non-OTG operation mode, VBus can not be turned off to take advantage of the power saving capability. The B-device will have the capability to initiate bus activity via SRP and hence the A-device will be capable of responding to this via SRP. The TD1120 On-The-Go port fully complies with the SRP protocol as described and defined in the USB On-The-Go specification.

Operational Modes: The TD1120 can be operated in different modes via software configuration:

	Peripheral port (P_DP, P_DM)	Port 1 (DP1, DM1)	Port 2 (DP2, DM2)	Application
On-The-Go and Host	OTG		Host	OTG application and one Host port (Concurrent OTG/Host operation supported. The OTG port may behave in either Host or Peripheral modes and dynamically switch between roles through the HNP, or when directed by a user by changing the USB cable connection)
Peripheral and Host	Peripheral	Host	Host	One high-speed Peripheral and two full-speed Hosts supporting simultaneous operation

Note: If using OTG application, then the TD1120 can be configured to support two ports, one Host and one OTG. When OTG is not utilized, then the TD1120 can be configured to support 3 ports, two Hosts and one Peripheral.

Microprocessor interface: The TD1120 is a memory mapped device that can gluelessly interface to the system bus of most popular microprocessors, CISC, RISC and DSPs including but not limited to x86, Intel XScale & StrongARM, Hitachi SH3, Fujitsu SPARCLite, NEC and Toshiba MIPS, ARM7, ARM9, Motorola PowerPC, ColdFire and Dragonball, among others. Reference designs and evaluation boards are available with new designs added and tailored to fit particular customer needs.

Software support: TransDimension is a leader in the USB embedded market, bringing both software and silicon to its customers. TransDimension provides development and support packages and a wide spectrum of USB host and On-The-Go software support in C source code to reduce development cost and time to market for its customers. Software for a variety of operating systems is fully tested and supported to easily interoperate with the above listed Microprocessors. TransDimension is a Microsoft Windows embedded partner.

TransDimension is a Microsoft Windows Embedded Partner (WEP) and supplies Host Controller Driver (HCD) Interface code to the TD1120 for Linux and WinCE operating systems, as well as applicable USB class and device drivers for use in a wide variety of mobile and post-PC products.

For many other Real Time Operating Systems (RTOS) as listed previously, TransDimension and SoftConnex supply the USBLink On-The-Go software solution, which utilizes proven software technologies from SoftConnex's USBLink Host and USBLink Device software products, thereby providing a complete, integrated solution for USB On-The-Go applications.

Pin Assignment and Definitions

LQFP Pin Assignment and Packaging

1	V _{SS}	26	NC	51	V _{SS}	76	DP ₂
2	D ₄	27	V _{SS}	52	NC	77	DM ₂
3	D ₅	28	A ₅	53	V _{DD2.5}	78	V _{DD3.3}
4	D ₆	29	A ₆	54	DP ₁	79	ENVREG
5	D ₇	30	A ₇	55	DM ₁	80	VREGOUT
6	V _{DD2.5}	31	V _{DDW}	56	V _{DD3.3}	81	V _{DD3.3A}
7	V _{DDW}	32	A ₈	57	V _{DD2.5}	82	V _{SSA}
8	D ₈	33	A ₉	58	/OC	83	V _{SS}
9	D ₉	34	A ₁₀	59	/EXVBO	84	V _{DD2.5}
10	D ₁₀	35	A ₁₁	60	VBP	85	V _{DDW}
11	D ₁₁	36	A ₁₂	61	/PO	86	/RESET
12	V _{SS}	37	ATEST13	62	ID	87	TEST
13	D ₁₂	38	NC	63	CLKCFG	88	GPIO
14	D ₁₃	39	/CS	64	XMODE	89	DRQ ₀
15	D ₁₄	40	V _{DD2.5}	65	V _{SS}	90	ACK ₀
16	D ₁₅	41	V _{SS}	66	V _{DD2.5}	91	EOT ₀
17	V _{DDW}	42	V _{SSA}	67	VOUT	92	DRQ ₁
18	V _{DD2.5}	43	V _{DD3.3A}	68	PD_PMOS	93	ACK ₁
19	INT	44	DP _P	69	V _{SSA}	94	EOT ₁
20	/WR	45	DM _P	70	V _{DD3.3A}	95	V _{DDW}
21	/RD	46	R _{REF}	71	EXT	96	D ₀
22	A ₁	47	V _{SSA}	72	VBUS	97	D ₁
23	A ₂	48	V _{DD3.3A}	73	V _{DD3.3A}	98	D ₂
24	A ₃	49	OSC ₂	74	V _{SSA}	99	D ₃
25	A ₄	50	OSC ₁	75	V _{SS}	100	V _{DD2.5}

Figure 2 - TD1120 pin assignment for the 100-pin LQFP 12x12mm

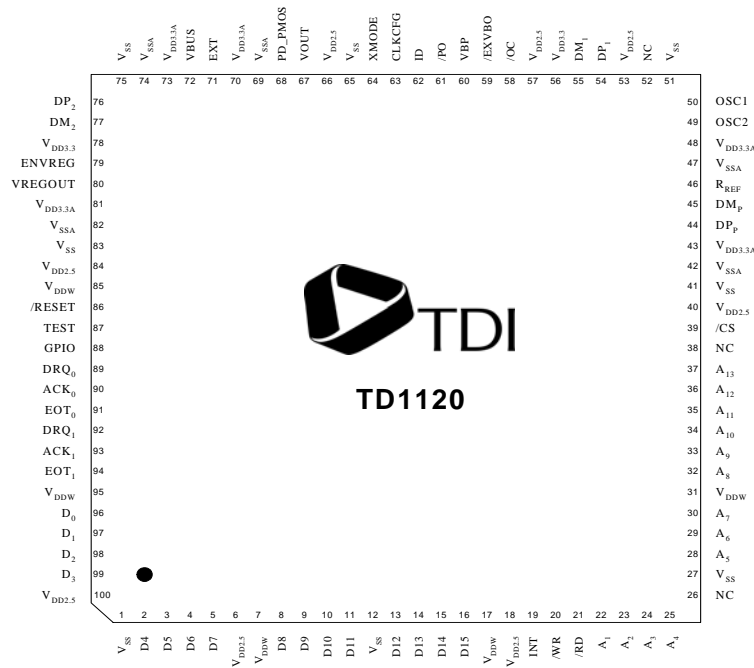


Figure 3 - TD1120 100-pin LQFP 12x12mm package (top view)

BGA Pin Assignment and Packaging

A1	D4	C1	D7	E1	D12	G1	/RD	J1	A4
A2	D3	C2	D8	E2	D13	G2	INT	J2	A3
A3	D0	C3	VSS	E3	VDD2.5	G3	/WR	J3	A7
A4	ACK1	C4	D1					J4	A9
A5	ACK0	C5	VDD2.5					J5	A12
A6	DRQ1	C6	VDD3.3					J6	/CS
A7	TEST	C7	DRQ0					J7	DPp
A8	VREGOUT	C8	VSS	E8	VSSA	G8	/EXVBO	J8	RREF
A9	DP2	C9	VDD3.3A	E9	PD_PMOS	G9	VBP	J9	OSC2
A10	DM2	C10	VSSA	E10	VOUT	G10	/PO	J10	DP1
B1	D5	D1	D9	F1	D15	H1	A1	K1	A6
B2	D6	D2	D10	F2	D14	H2	A2	K2	A5
B3	D2	D3	D11	F3	VDDW	H3	VDD2.5	K3	A8
B4	EOT1					H4	A10	K4	A11
B5	EOT0					H5	VDDW	K5	ATEST13
B6	/RESET					H6	VSS	K6	VSSA
B7	GPIO					H7	VDD3.3A	K7	DMp
B8	ENVREG	D8	VBUS	F8	ID	H8	VDD3.3	K8	VSSA
B9	VDD3.3A	D9	VDD3.3A	F9	CLKCFG	H9	DM1	K9	VDD3.3A
B10	VSSA	D10	EXT	F10	XMODE	H10	/OC	K10	OSC1

Figure 4 - TD1120 pin assignment for the 84-ball BGA 7x7mm

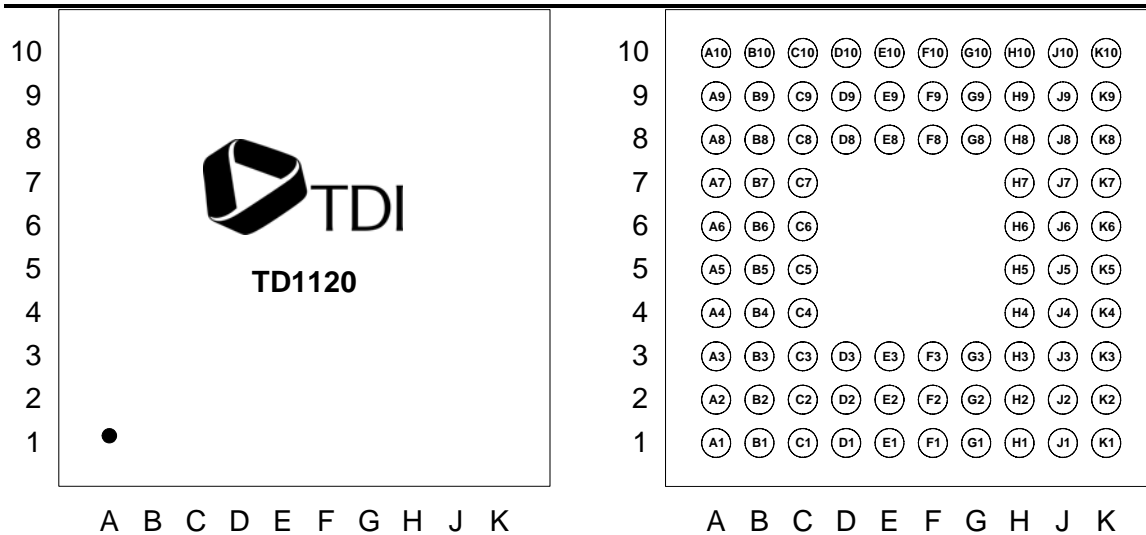


Figure 5 - TD1120 84-ball BGA 7x7mm package (top views)

Pin Definitions

The following notations are used to indicate the type of a signal/pin:

I	INPUT	O	OUTPUT	PL	ACTIVE LEVEL PROGRAMMABLE
IO	BI-DIRECTIONAL	WO	WIRED OR	NA	NOT APPLICABLE
PW	POWER/GROUND	PS	PASSIVE	NC	NO CONNECT
H	ACTIVE HIGH	L	ACTIVE LOW		

Pin/Signal Name	Signal Type	Active Level	Voltage Level	Pin/Signal Description
OSC ₁	I		V _{DD3.3A}	A 12 MHz or 30 MHz passive crystal should be connected across the two pins. Optionally, a 12 MHz or 30 MHz Oscillator can be sourced through OSC1 while keeping OSC2 unconnected.
OSC ₂	O			
/RESET	I	L	V _{DDW}	Hardware reset.
/CS	I	L	V _{DDW}	Chip select.
/MR	I	L	V _{DDW}	Write strobe.
/RD	I	L	V _{DDW}	Read strobe.
A ₁₂ :A ₁	I		V _{DDW}	Address bus for direct address space of 8K bytes.
D ₁₅ :D ₀	IO		V _{DDW}	16-bit data bus.
DRQ ₁ :DRQ ₀	O	PL	V _{DDW}	DMA Request outputs to support 2 channels
ACK ₁ :ACK ₀	I	PL	V _{DDW}	DMA Acknowledge
EOT ₁ :EOT ₀	I	PL	V _{DDW}	Optional DMA End Of Transfer indicator
INT ¹	O/WO	PL	V _{DDW}	Interrupt to the MCU. This pin can be software configured as a regular output or WO. (WO is the default).

¹ The active level for INT is programmable by software but defaults to active low after power on or hardware reset. This feature allows glue-less interfacing with most microprocessors. Caution must be taken in user software to make sure relevant operations (interrupt) are disabled before alterations to default active levels are made.

GPIO	IO	PL	V _{DDW}	General Purpose IO.						
CLKCFG	I		V _{DD3.3}	The state of this pin is used to indicate whether a 12MHz or a 30MHz Crystal/Oscillator is being used. <table border="1" data-bbox="678 279 1263 478"> <thead> <tr> <th>CLKCFG</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>12 MHz Crystal 12 MHz 3.3V Oscillator input on OSC1</td> </tr> <tr> <td>1</td> <td>30 MHz Crystal 30 MHz 3.3V Oscillator input on OSC1</td> </tr> </tbody> </table>	CLKCFG	Frequency	0	12 MHz Crystal 12 MHz 3.3V Oscillator input on OSC1	1	30 MHz Crystal 30 MHz 3.3V Oscillator input on OSC1
CLKCFG	Frequency									
0	12 MHz Crystal 12 MHz 3.3V Oscillator input on OSC1									
1	30 MHz Crystal 30 MHz 3.3V Oscillator input on OSC1									
DM _P , DP _P	IO		V _{DD3.3}	Data lines for <i>USB Peripheral Port</i> , which may serve as an OTG port in combination with Host Port 1. If not used, these two pins should be left floating.						
DM ₁ , DP ₁	IO		V _{DD3.3}	Data lines for Host Port 1, which may serve as a <i>USB Host</i> or an OTG port in combination with the Peripheral Port. If not used, these two pins should be left floating.						
DM ₂ , DP ₂	IO		V _{DD3.3}	Data lines for Host Port 2, a dedicated <i>USB Host</i> port. If not used, these two pins should be left floating.						
/PO	O	L	V _{DD3.3}	Turn on/off the gang power for all Host ports.						
/OC	I	L	V _{DD3.3}	Over current condition indicator for gang powered Host ports.						
ID	I		V _{DD3.3}	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, it determines the chip's responsibility in an OTG application, (0: A-DEVICE, 1: B-DEVICE). For non-OTG application, this pin should be left floating.						
/EXVBO	O	L	V _{DD3.3}	Turn on/off the external V _{BUS} (5V) for OTG operation (1: V _{BUS} off; 0: V _{BUS} on) when using the external Chargepump.						
VBUS	I			V _{BUS} input used by the Peripheral port for connection; and also sampled during HNP/SRP operations when used as an OTG port. This pin should be left floating in a Host only application.						
VBP	IO	H	V _{DD3.3}	V _{BUS} pulsing control. This pin is used only OTG port is operating as a B-DEVICE.						
EXT	O	H	V _{DD3.3A}	Internal Chargepump output for N-MOSFET (Refer Section TBD)						
PD_PMOS	O		V _{DD3.3A}	Internal Chargepump output for P-MOSFET (optional switch on the VOUT)						
VOUT	I			Internal Chargepump output voltage feedback pin						
R _{REF}	IO		V _{DD3.3A}	Connect external reference resistor (12 kΩ ± 1%) to V _{SSA} .						
ENVREG	I		V _{DD3.3A}	Enables the internal Voltage Regulator if asserted. If not used, this pin should be tied to V _{SS} .						
VREGOUT	PW			Internal Voltage Regulator output of 2.5V If enabled, this output should be connected to the V _{DD2.5} , V _{DD2.5A} (and V _{DDW} if Wide-range IO is at 2.5V) supplies of the chip. If the Regulator is disabled, then this pin should be treated as another V _{DD2.5} supply input to the chip.						
XMODE	I	H	V _{DD3.3}	This pin should be grounded for normal operation.						
TEST	I	H	V _{DDW}	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation.						
ATEST13	I		V _{DDW}	Additional address pin for debug usage. Should be grounded or left						

				floating (has an internal pull-down) for normal operation.
$V_{DD3.3A}$	PW			Analog +3.3V.
V_{SSA}	PW			Analog ground.
$V_{DD3.3}$	PW			Digital +3.3V.
$V_{DD2.5}$	PW			Digital +2.5V.
V_{DDW}	PW			Wide-range IO +2.5V to +3.3V.
V_{SS}	PW			Digital/Wide-range IO ground.
NC	PS			No connection. These pins should be left floating.

Table 1 - TD1120 pin/signal description

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD3.3}$	3.3V Power Supply		-0.3	3.9	V
$V_{DD2.5}$	2.5V Power Supply		-0.3	3.0	V
V_{DDW}	2.5V to 3.3V Power Supply		-0.3	3.9	V
V_I	DC input voltage		-0.3	5.5	V
T_S	Storage temperature		-40	+150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the Normal Operating Conditions specified in the following section. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended/Normal Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD3.3}$	3.3 V Power Supply		3.0	3.6	V
$V_{DD2.5}$	2.5 V Power Supply		2.25	2.75	V
V_{DDW}	2.5 – 3.3 V Wide-range I/O Power Supply		2.25	3.6	V
$V_{I3.3}$	DC input voltage of 3.3V pins		0	3.6	V
V_{IW}	DC input voltage of Wide-range pins		0	$V_{DDW} + 0.3$	V
I_{DDH}	Host Operational Current	ENVREG = 1	TBD	36	mA
I_{DDF}	Peripheral Operational Current	High-speed, ENVREG = 1	TBD	80	mA
		Full-speed ENVREG = 1	TBD	58	mA
I_{DDHS}	Host Suspend State Current	ENVREG = 1	TBD	TBD	μA

I_{DDFS}	Peripheral Suspend State Current	ENVREG = 1	360	480	μA
I_{DDPS}	Power Save State Current	ENVREG = 1	110	220	μA
		ENVREG = 0	TBD	TBD	μA
T_O	Operating temperature		-40	+85	$^{\circ}\text{C}$

Note: The operational current measurements are made under average bus traffic condition with typical parts at room temperature. The actual current may be slightly higher or lower depending upon the application.

D.C. Characteristics

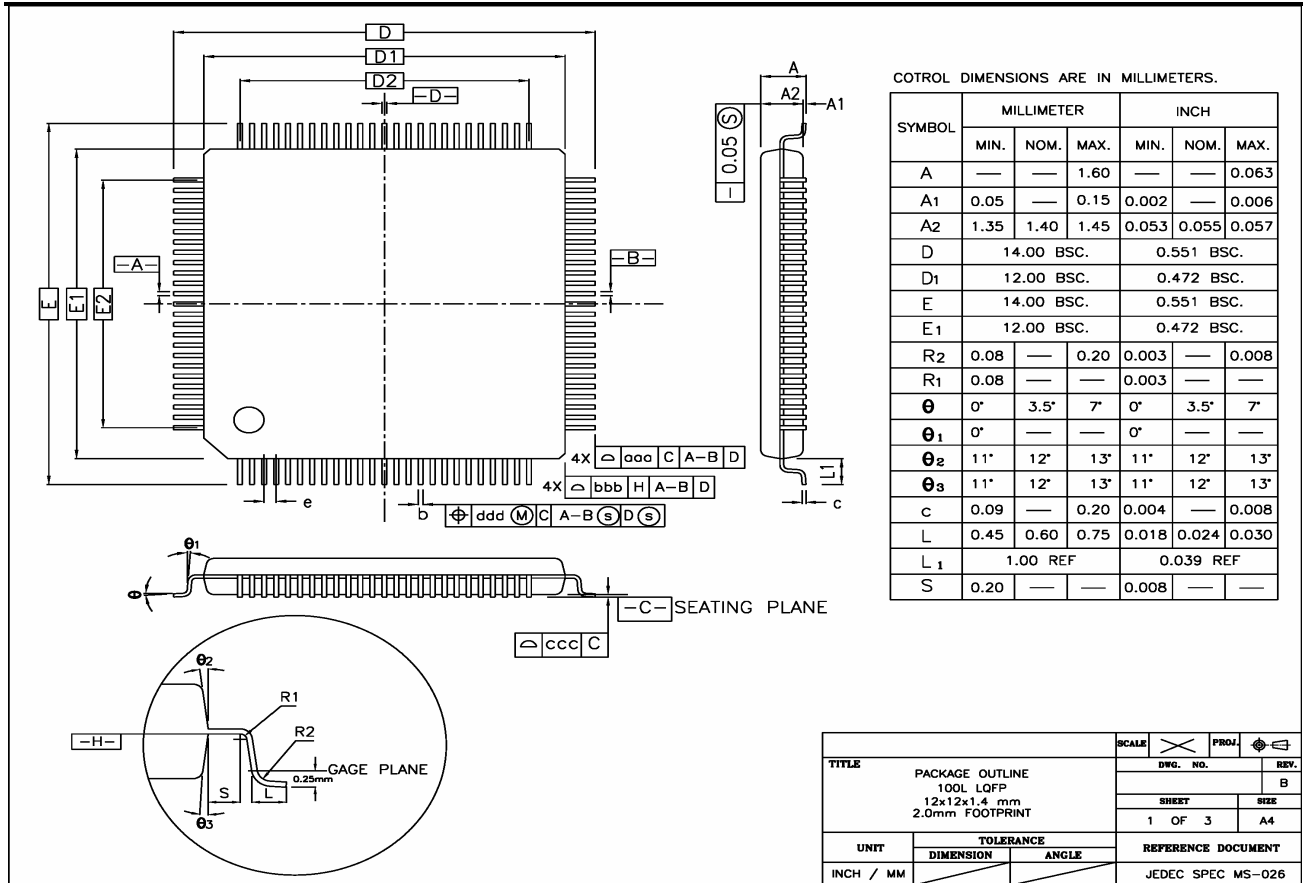
USB I/O Signals: DP_n , DM_n (for Full-speed Host)

Symbol	Parameter	Condition	Min	Max	Unit
V_{DI}	Diff. Input Sensitivity	DP_n and DM_n	0.2		V
V_{CM}	Diff. Comm. Mode Range		0.8	2.5	V
V_{OL}	Static Output Low			0.3	V
V_{OH}	Static Output High		2.8		V
V_{CRS}	Output Signal Crossover		1.3	2.0	V
C_{IN}	Input Capacitance			20	pF

Logic Signals

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low level output voltage			0.4	V
V_{OH}	High level output voltage	$V_{DDW} = 3.3\text{ V}$	2.4		V
		$V_{DDW} = 2.5\text{ V}$	2.0		V
V_{IL}	Low level input voltage	$V_{DDW} = 3.3\text{ V}$		0.8	V
		$V_{DDW} = 2.5\text{ V}$		0.7	V
V_{IH}	High level input voltage	$V_{DDW} = 3.3\text{ V}$	2.0		V
		$V_{DDW} = 2.5\text{ V}$	1.7		V
C_{IN}	Input Capacitance		3.1 (typical)		pF
C_{OUT}	Output Capacitance		3.1 (typical)		pF
C_{BI}	Bi-directional Capacitance		3.1 (typical)		pF
I_{IN}	Input leakage current	No pull up or pull down	-10	10	μA

Note: The capacitances listed above do not include PAD capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance, which is about 0.1 pF; and the package capacitance, which is about 0.86 pF max for QFP.



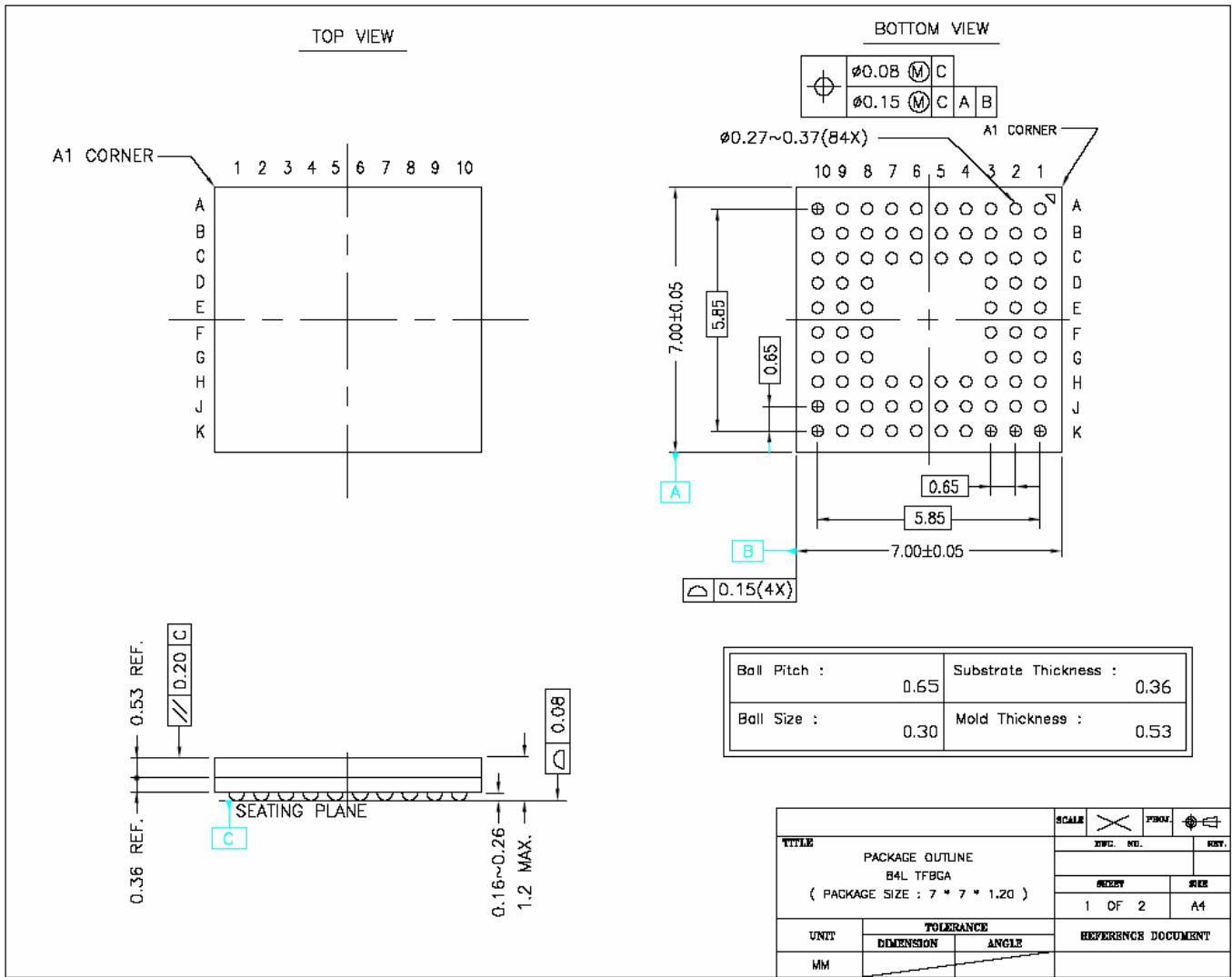
SYMBOL	100L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	9.60			0.378		
E2	9.60			0.378		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

UNIT	TOLERANCE		REFERENCE DOCUMENT
	DIMENSION	ANGLE	
INCH / MM			JEDEC SPEC MS-026

LQFP-100pin 12x12mm Packaging & Dimensions



BGA-84balls 7x7mm Packaging & Dimensions

Applicable Documents and Specifications

- ❑ On-The-Go supplement to the USB 2.0 specification, Revision 1.0, Dec 18, 2001.
URL Link: http://www.usb.org/developers/data/otg1_0.pdf
- ❑ USB 2.0 specification, URL Link: http://www.usb.org/developers/data/usb_20.zip
- ❑ USB On-The-Go Marketing Overview, Feb 26, 2002. URL Link:
http://www.usb.org/data/developers/otg/presentations/london/OTG_marketing.pdf

Ordering information

Silicon	Pin/Ball Number	Package Type	TransDimension Order Number
TD1120 Silicon – Leaded (Pb)	84 balls	TF-BGA	TDOTG1120-00BC
	100 pins	LQFP	TDOTG1120-000C
TD1120 Silicon – Lead Free (Pb free)	84 balls	TF-BGA	TDOTG1120-0FBC
	100 pins	LQFP	TDOTG1120-0F0C

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