



PCI 9030AA Data Book Addendum

A. Affected Silicon Revision

This document details addendum documentation for the following silicon:

Product	Revision	Description	Status
PCI 9030	AA	PCI SMARTarget I/O Accelerator	Production

B. Documentation Version

The following documentation details the silicon baseline functional description:

Document	Version	Description	Publication Date
<i>PCI 9030 Data Book</i>	1.4	Data Book	September 2004

C. Addendum Documentation Revision History

Revision	Date	Description
1.0	7/12/05	Baseline.
1.1	10/25/05	Added item 20 , Addendum to PCN 2005-4.
1.2	03/24/06	Added item 21 , EOL of PCI9030-AA60VPI and package dimensions of PCI9030-AA60PI F.

D. Addendum Documentation Summary

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1. PCI 9030 Lead-Free ROHS-Compliant Version Ordering Information

The PCI 9030 is available in standard leaded packaging and lead-free ROHS packaging. Ordering information is delineated in the following table.

Part Number	Package
PCI 9030-AA60PI	Standard Leaded PQFP Package
PCI 9030-AA60PI F	Lead-Free ROHS PQFP Packaging
PCI 9030-AA60BI	Standard Leaded BGA Package
PCI 9030-AA60BI F	Lead-Free ROHS BGA Packaging

2. Local Address Setup Time Prior to ADS#/ALE Assertion

The *PCI 9030 Data Book*, v1.4, Section 2.2.4.1, "Bus Cycles," on page 2-6 states:

"In both Non-Multiplexed and Multiplexed modes, the LA[27:2] Address Bus drives an access address valid beginning one clock prior to ADS# assertion (which signals the start of the Bus cycle) and continues until the cycle ends (signaled by BLAST# de-assertion). In Multiplexed mode (MODE=1), the LAD/LD[31:0] Multiplexed Address/Data Bus also drives the access address valid onto LAD/LD[27:0], beginning one clock prior to ADS# assertion and continuing until ADS# de-assertion one clock later, after which data is driven."

This description incorrectly indicates that the Local Address is driven valid, beginning one clock prior to ADS# assertion. The Local Address is driven zero to two clocks prior to ADS# or ALE assertion, and therefore external logic should not decode the Local Address until ADS# or ALE is asserted.

The two sentences in the *PCI 9030 Data Book*, v1.4, are being replaced with the following description:

"In both Non-Multiplexed and Multiplexed modes, the LA[27:2] Address Bus and LBE[3:0]# Byte Enables drive an access address valid, beginning zero to two clocks prior to ADS# assertion (which signals the start of the Bus cycle) and continues until the cycle ends (signaled by BLAST# de-assertion). In Multiplexed mode (MODE=1), the LAD/LD[31:0] Multiplexed Address/Data Bus also drives the access address valid onto LAD/LD[27:0], beginning zero to two clocks prior to ADS# assertion and continuing until ADS# de-assertion one clock later, after which data is driven. External logic should not decode the Local Address and Byte Enables until ADS# or ALE is asserted."

3. Reloading Registers from Serial EEPROM

The *PCI 9030 Data Book*, v1.4, Section 3.3, “Serial EEPROM,” on page 3-1, includes the following paragraph:

“To reload serial EEPROM data into the PCI 9030 internal registers, write 1 to the Reload Configuration Registers bit (CNTRL[29]=1).”

Append the following sentence to this paragraph:

“This bit is **not** self-clearing.”

4. Recommended Serial EEPROMs

The *PCI 9030 Data Book*, v1.4, Section 3.3.1.2, “Recommended Serial EEPROMs,” on page 3-2 refers to the serial EEPROM Guidelines document posted at <http://www.plxtech.com/products/default.htm>.

The correct URL is http://www.plxtech.com/products/io_accelerators/.

5. Serial EEPROM Offset 08h

The *PCI 9030 Data Book*, v1.4, Table 3-2, “Serial EEPROM Register Load Sequence,” on page 3-3, under Serial EEPROM offset 08h, should state “PCICCR[23:8]” instead of “PCICCR[15:0]”.

6. Internal Register Access

The *PCI 9030 Data Book*, v1.4, Section 3.4, “Internal Register Access,” on page 3-6 incorrectly states:

“These registers are accessible from the PCI and Local Buses,” which, as internal registers cannot be directly accessed from the Local Bus.”

This sentence is replaced by the following text:

“These registers are accessible from the PCI Bus; registers are not accessible from the Local Bus because the LA[28:2] and LBE[3:0]# signals are always outputs. Registers are modified only from the Local Bus, when any of the following conditions are met:

- GPIO pins configured as inputs, reflecting pin voltage level in the corresponding GPIOC register Data bits
- Local Interrupt input LINT[2:1] levels, reflecting pin voltage level in the Interrupt Status bits INTCSR[5, 2]

- CPCISW input toggling, affecting the Hot Swap HS_CSR[7, 6] states
- Serial EEPROM interface EEDO input, reflecting pin voltage level in the Read Serial EEPROM Data bit (CNTRL[27])

Additionally, Figure 3-2 details interrupt access; however, its title, “PCI 9030 Internal Register Access,” implies register access. Replace the figure title with the following:

Figure 3-2. “PCI 9030 Register Access from PCI and Interrupt Options”

7. CNTRL[15] Relationship with CNTRL[14]

The *PCI 9030 Data Book*, v1.4, Section 4.2.1.2.3, “PCI r2.2 16- and 8-Clock Rule,” on page 4-2 indicates that PCI Read with Write Flush mode (CNTRL[15]=1) is enabled only if both this bit and the *PCI 2.2* Features Enable bit is set (CNTRL[14]=1). However, setting CNTRL[15] enables PCI Read with Write Flush mode regardless of the *PCI 2.2* Features Enable bit value (CNTRL[14]=0 or 1). Setting the *PCI 2.2* Features Enable bit is recommended to avoid possible violation of the PCI 16-clock and 8-clock latency rules, made mandatory with *PCI 2.1* and later. PCI Read with Write Flush mode should not be enabled without the *PCI 2.2* Features Enable bit set.

8. Invalid Timing Diagram 4-32

The information presented in the *PCI 9030 Data Book*, v1.4, Timing Diagram 4-32, “PCI Target Non-Burst Read, Non-Multiplexed Mode Only,” on page 4-37, is incorrect. Therefore, the timing diagram is being removed from the *PCI 9030 Data Book*, v1.4.

9. Three-State I/O Pins Configured as Outputs Float Immediately upon LREQ Input Assertion

a. The *PCI 9030 Data Book*, v1.4, Section 6.3, “General Purpose I/O”, on page 6-3, includes the following paragraph:

“GPIO[8:0] pins configured as outputs are driven only when the PCI 9030 owns the Local Bus. (Refer to *PCI 9030 Errata #2*.)”

Replace this paragraph with the following text:

“GPIO[8:0] pins configured as outputs are driven only when the PCI 9030 owns the Local Bus, and float immediately upon LREQ input assertion. (Refer to *PCI 9030 Errata #2*.)”

b. In the *PCI 9030 Data Book*, v1.4, below Register 10-60, “(GPIOC; 54h) General Purpose I/O Control,” on page 10-37, a Note is included that states:

“Note: GPIO pins configured as outputs are driven only when the PCI 9030 owns the Local Bus. When another local master owns the bus (LGNT asserted), GPIO pins configured as outputs are floated. (Refer to PCI 9030 Errata #2 for additional information.)”

Replace the Note with the following text:

“Note: GPIO pins configured as outputs are driven only when the PCI 9030 owns the Local Bus and LREQ input is not asserted. When another local master requests the bus (LREQ input asserted) or owns the bus (LGNT output asserted), GPIO pins configured as outputs are floated. (Refer to PCI 9030 Errata #2 for additional information.)”

c. The *PCI 9030 Data Book*, v1.4, the Table 11-4, “I/O Pin Pull-Up and Pull-Down Resistor Requirements,” **Requirements** column on page 11-3, includes a Note for the GPIO0/WAITo#, GPIO1/LLOCKo#, GPIO2/CS2#, GPIO3/CS3#, GPIO4/LA27, GPIO5/LA26, GPIO6/LA25, GPIO7/LA24, GPIO8 pins that states:

“Note: Refer to PCI 9030 Errata #2, regarding the GPIO[8:0] pins which, when configured as outputs, are floated when the PCI 9030 does not own the Local Bus.”

Replace the Note with the following text:

“Note: Refer to PCI 9030 Errata #2 and #10, regarding the GPIO0/WAITo#, GPIO1/LLOCKo#, GPIO2/CS2#, GPIO3/CS3#, GPIO4/LA27, GPIO5/LA26, GPIO6/LA25, GPIO7/LA24, GPIO8 pins which, when configured as outputs (that is, not configured as GPIO inputs), are floated when the PCI 9030 does not own the Local Bus and/or when LREQ input is asserted.”

10. Hot Swap Next Capability Pointer Value

a. The *PCI 9030 Data Book*, v1.4, Section 8.2.2.4, “Hot Swap Capabilities Register” on page 8-4, includes the following paragraph:

Next_Cap Pointer. Bits [15:8] (HS_NEXT[7:0]; PCI:49h). These bits either point to the next New Capability structure, or are set to 0h if this is the last capability in the structure. Bits [9:8] are **reserved** by PCI r2.2, and should be set to 00.”

Replace the paragraph with the following text:

Next_Cap Pointer. Bits [15:8] (HS_NEXT[7:0]; PCI:49h). These bits point to the next New Capability structure. These bits must always contain the default value 4Ch. (Refer to *PCI 9030 Errata #9*.)”

b. In the *PCI 9030 Data Book*, v1.4, Register 10-32, “(HS_NEXT; PCI:49h) Hot Swap Next Capability Pointer,” description on page 10-32, the last sentence states:

“If Hot Swap is the last capability in the list, set to 0h.”

Replace the sentence with the following text:

Note: *These bits must always contain the default value 4Ch. (Refer to PCI 9030 Errata #9.)*

11. Table 10-5 PCI Writable Bits for Offset 4Ch

The PCI Writable bits listed in the *PCI 9030 Data Book*, v1.4, Table 10-5, “Control Register Address Mapping,” on page 10-3, is incorrect. The writable bits, currently listed as “[31:8]” should be “[23:0]”.

12. Next Capability Pointer Value

In the *PCI 9030 Data Book*, v1.4, Register 10-20, “(CAP_PTR; PCI:34h) New Capability Pointer,” description on page 10-10, remove the sentence “Bits [1:0] are **reserved** by *PCI r2.2*, and should be set to 00 (the byte value points to an Lword boundary.”

13. Power Management Next Capability Pointer Value

The *PCI 9030 Data Book*, v1.4, Register 10-26, “(PMNEXT; PCI:41h) Power Management Next Capability Pointer,” description on page 10-12, includes the following text:

“Bits [1:0] are **reserved** by *PCI r2.2*, and should be set to 00 (the byte value points to an Lword boundary). If Power Management is the last capability in the list, set to 0h.”

Replace these two sentences with the following text:

Note: *These bits must always contain the default value 48h. (Refer to PCI 9030 Errata #9.)*

14. INTCSR[11:10] Descriptions, Offset 4Ch

Append the following sentence to the INTCSR[11:10] bit descriptions in the *PCI 9030 Data Book*, v1.4, Register 10-57, “(INTCSR; 4Ch) Interrupt Control Status,” on page 10-33:

“This bit is self-clearing.”

15. CNTRL[31:29,18,14] Descriptions, Offset 50h

a. Append the following sentence to the CNTRL[14] bit description in the *PCI 9030 Data Book, v1.4*, Register 10-59, “(CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control,” on page 10-34:

Note: *Value of 1 is recommended for compliance to the PCI r2.2 16- and 8-clock target latency rules.*

b. Append the following sentence to the CNTRL[18] bit description in the *PCI 9030 Data Book, v1.4*, Register 10-59, “(CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control,” on page 10-34:

Note: *Value of 1 is recommended, so that in case the Write FIFO fills after the initial data phase of a burst write, and after 7 PCI wait states (TRDY# de-asserted) it remains full (because the local bus target has not accepted data), the PCI 9030 will disconnect (assert STOP#) in compliance to the PCI 8-clock target latency rule, rather than continue to hold the PCI Bus with wait states.*

c. Append the following sentence to the CNTRL[30:29] bit descriptions in the *PCI 9030 Data Book, v1.4*, Register 10-59, “(CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control,” on page 10-35:

“This bit is **not** self-clearing.”

d. The CNTRL[31] bit description states:

“Disconnect with Flush Read FIFO. When the *PCI r2.2* Features Enable bit is set (bit [14]=1), value of 1 causes acceptance of a new Read request with flushing of the Read FIFO when a PCI Target Read request does not match an existing, pending Delayed Read in the Read FIFO. Value of 0, or clearing of the *PCI r2.2* Features Enable bit (bit [14]=0), causes a new Target Read request (different command, address and/or byte enables) to be Retried when a Delayed Read is pending in the Read FIFO.”

Replace the CNTRL[31] bit description with the following text:

“Disconnect with Flush Read FIFO. When the *PCI r2.2* Features Enable bit is set (bit [14]=1) during a Delayed Read completion, after at least one datum of a burst is transferred, if the master continues to request additional data but the Read FIFO is empty of local bus data for 7 PCI wait states (TRDY# de-asserted), the PCI 9030 issues a Disconnect Without Data in compliance with the *PCI r2.2* 8-clock latency rule, which requires that subsequent data of a burst be available within 8 PCI clocks of the previous Data phase.

When the *PCI r2.2 Features Enable* bit is set (bit [14]=1), value of 1 causes acceptance of a new Read request with flushing of the Read FIFO when the new PCI Target Read request does not match the next sequential address for data at which the PCI 9030 terminated its bursting of data for an immediately preceding Delayed Read completion, by a Disconnect Without Data.

Value of 0, or clearing of the *PCI r2.2 Features Enable* bit (bit [14]=0), causes a new Target Read request (different command, address and/or byte enables) to be Retried when a PCI Target Read request does not match the next sequential address at which the PCI 9030 terminated the burst of an immediately preceding Delayed Read completion, by a Disconnect Without Data.

Note: *Recommended value is 1 for PCI r2.2 compliance, particularly if the Memory space is mapped as Prefetchable (PCIBARx[3]=1), in which case an upstream bridge might resume the read at the previous Qword boundary after discarding the last Lword that was read if its address was not Qword-aligned.*

16. Table 11-2 JTAG-Related Content

The JTAG TCK, TDI, and TMS pin information provided in the *PCI 9030 Data Book*, v1.4, Table 11-2, “Input Pin Pull-Up and Pull-Down Resistor Requirements,” on page 11-2, is incorrect. Replace the entire description with the following text:

“If JTAG is not used, tie TCK high and tie TDI and TMS low. If used, per the *IEEE 1149.1 Specification*, an external pull-up is required on the TDI and TMS signals.”

Also, remove the following phrase from the table’s Note:

“therefore, the pull-up resistors must be added externally to the PCI 9030.”

Additionally, append a second note to the table that states:

“Per *PCI r2.2*, PCI expansion boards that do not implement JTAG Boundary Scan must connect PCI Connector signals TDI and TDO together so that the system scan chain is not broken. For CompactPCI, use of JTAG signals is discouraged per *PICMG 2.0 R3.0*.”

Note: *The pin descriptions provided in Table 11-8, “Test and Debug Pins,” on page 11-6 are **not** affected by the changes applied to Table 11-2.*

17. VIO Pin Description

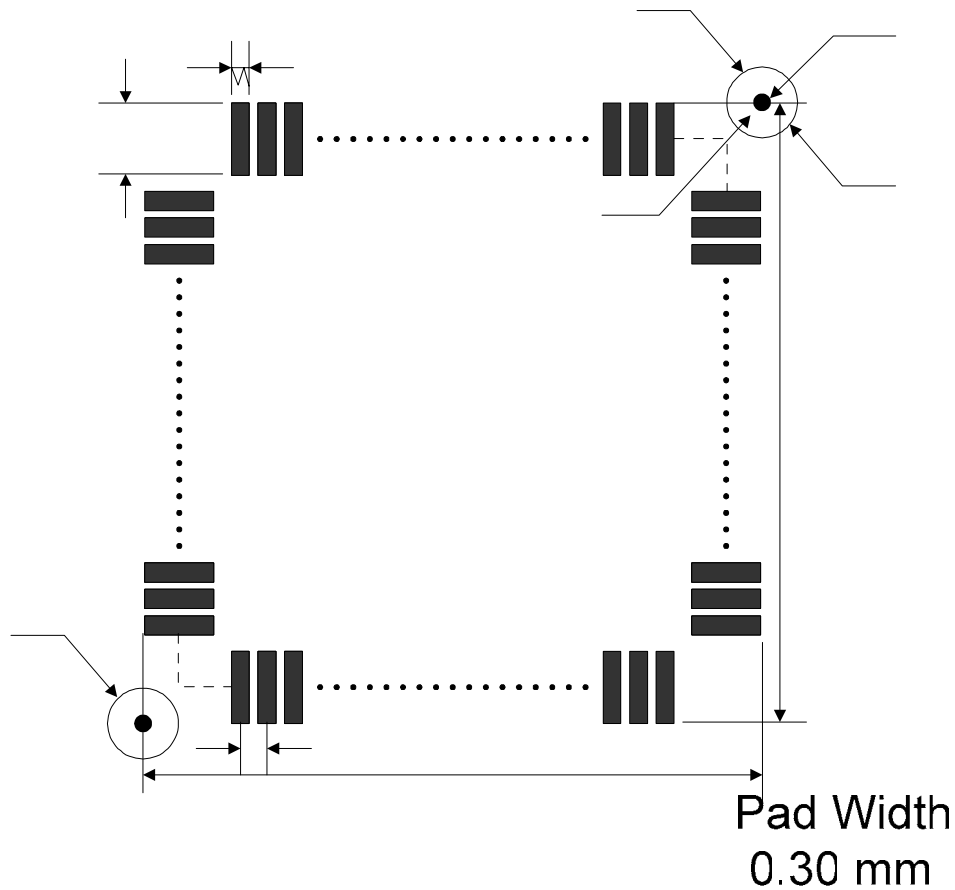
The *PCI 9030 Data Book*, v1.4, Tables 11-5 and 11-6, which list the Power and Ground connections, also include the VIO power pin. In the **Function** column of these tables, append the following description for VIO:

VIO is the common cathode of the upper clamp diodes that have anodes connected to each of the PCI I/O buffers, providing a discharge path for protection from overvoltage conditions [voltage spikes, surges, and electrostatic discharge (ESD)] that exceed the signaling environment voltage (5 or 3.3V) defined by the motherboard. VIO must be connected to 5V in a 5V signaling environment, or to 3.3V in a 3.3V signaling environment. When designing Universal PCI add-in cards (that can plug into either 3.3 or 5V slots), the VIO pin must be connected to one or more of the PCI connector VIO pins. Refer to the *PCI r2.2*, Section 4.4.2.1, for VIO decoupling requirements.

18. Figure 13-2 Land Pattern Dimensions

The *PCI 9030 Data Book*, v1.4, Figure 13-2, “176-Pin PQFP PCB Layout Suggested Land Pattern,” on page 13-2, indicates incorrect dimensions. The following table lists the old and new values, and the illustration replaces the current Figure 13-2.

Figure 13-2 Label	Old Value	New Value
Pad Width	0.3048	0.30
Pad Length	1.524	1.50
Metal Pad	1.016	1.00
A	27.178	27.18
B	27.178	27.18



Pad Length
1.50 mm

19. Table 13-5 μ BGA Layout Information Being Removed

The PCI 9030 Data Book, v1.4, Table 13-5, "180-Pin μ BGA Six-Layer Board Routing Example (Four Routing Layers)—Sample Parameters," on page 13-7 is intended to list sample dimensions for board layout. The dimensions included in this table are incorrect for board layout, and therefore Table 13-5 is being removed from the *PCI 9030 Data Book*. Designers should consult with their board assembly house to obtain recommended layout parameters.

20. Addendum to PCN 2005-4

PCI9030-AA60PI devices are no longer being manufactured in body size 24 x 24 x 2.7 mm (QFP18). These devices are being replaced with body size 24 x 24 x 1.4 mm (QFP21) devices, and will be offered with a new ordering code, PCI9030-AA60VPI.

21. EOL of PCI9030-AA60VPI and package dimensions of PCI9030-AA60PI F

The PCI9030-AA60VPI has gone into EOL stage with a Last time buy date of 09/15/2006 and a last time ship date of 03/30/2007. However PLX will continue to ship the lead-free version PCI9030-AA60PI F and the package dimensions of this lead-free device are 24 x 24 x 1.4 mm (QFP21).

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