

ExpressLane PEX 8524

Flexible & Versatile PCI Express™ Switch

Features

- **PEX 8524 General Features**
 - 24-lane PCI Express switch
 - Integrated SerDes
 - Up to six configurable ports (x1, x2, x4, x8)
 - 35mm x35mm, 680 pin PBGA package
 - Typical Power: 4.1 Watts
- **PEX 8524 Key Features**
 - Standards Compliant
 - PCI Express Base Specification, r1.0a
 - PCI Standard SHPC Specification, r1.1
 - High Performance
 - Non-blocking Switch Fabric
 - Full Line rate
 - Configurable **Non-transparent** port for Multi-Host or Intelligent I/O Support
 - Flexible Configuration
 - Eight highly flexible and configurable ports
 - Flexible lane width/port x1, x2, x4, x8
 - Configurable with strapping pins, EEPROM, or Host software
 - Lane and polarity reversal
 - PCI Express Power Management
 - Link power management states: L0, L0s, L1, L2/L3 Ready, and L3
 - Device states: D0 and D3hot
 - Quality of Service (QoS)
 - **Two Virtual Channels** per port
 - Eight Traffic Classes per port
 - Fixed and round robin Virtual Channel arbitration
 - Reliability, Availability, Serviceability (RAS)
 - Standard Hot-Plug Controller
 - Upstream port as hot-plug client
 - Transaction Layer **end-to-end CRC**
 - Poison bit
 - Error reporting in addition to advanced error reporting support of PCI Express
 - Per port performance monitoring
 - Average packet size, number of packets, CRC errors
 - JTAG boundary scan



Multi-purpose and Feature Rich PCI Express* ExpressLane™ Switch

The ExpressLane **PEX 8524** device offers PCI Express **switching** capability conforming to the latest revision of the PCI Express Base specification. This device enable users to add scalable high bandwidth, **non-blocking** interconnection to a wide variety of applications including servers, storage systems, communications platforms, blade servers, and embedded-control products. The PEX 8524 switch can be used as **fanout**, **aggregation**, **dual graphics**, or **peer-to-peer** switching, and is equally well-suited for **intelligent I/O** module applications.

Highly Flexible Port Configurations

The ExpressLane PEX 8524 offers highly configurable ports. There are a maximum of 6 **ports** that can be configured to any legal width from x1 to x8, in any combination to support your specific bandwidth needs. The ports can be **symmetric** (each port having the same lane width) or **asymmetric** (ports having different lane widths). *If you can think of a port/lane combination, you can configure it!* **Any** of the ports can be designated as the **upstream** port, and you can even dynamically change the upstream port.

End-to-end Packet Integrity

The ExpressLane PEX 8524 provides **end-to-end CRC** protection (ECRC) and **Poison** bit support to enable designs that require **guaranteed error-free packets**. These features are optional in the PCI Express specification, but PLX provides them across its entire ExpressLane switch product line.

Non-Transparent “Bridging” in a PCI Express Switch

The ExpressLane PEX 8524 product supports full non-transparent bridging functionality to allow implementation of multi-host systems and intelligent I/O modules in applications such as **communications**, **storage**, and **graphics fanout**. To ensure quick product migration, the non-transparency features are implemented in the same fashion as in standard PCI applications.

Non-transparent bridges allow systems to isolate memory domains by presenting the processor subsystem as an endpoint, rather than another memory system. Base address registers are used to translate addresses; doorbell registers are used to send interrupts between the address domains; and scratchpad registers are accessible from both address domains to allow inter-processor communication.

Two Virtual Channels

The ExpressLane PEX 8524 switch supports 2 full-featured Virtual Channels (VCs) and **8 Traffic Classes (TCs)**. The mapping of Traffic Classes to port-specific Virtual Channels allows for different mappings on different ports. In addition, the devices offer user-selectable Virtual Channel arbitration algorithms to enable users to fine tune the Quality of Service (QoS) required for a specific application.

Low Power with Granular SerDes Control

The ExpressLane PEX 8524 provides **low power** capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be **turned off** when unused for even lower power.

Flexible Port Width Configuration

The lane width for each port can be individually configured through auto-negotiation, hardware strapping, upstream software configuration, or through an optional EEPROM.

The ExpressLane PEX 8524 supports a large number of port configurations. For example, if you are using the PEX 8524 in a fan-out application (such as in Figure 1), you may configure the upstream port as x8 and the downstream ports as four x4 ports; three x8 ports; or **any other combination** as long as you don't run out of lanes or ports. For a peer-to-peer application, you can configure all six ports as x4 or x2, or a combination of the two. In a port aggregation application you can configure four x2 or x4 ports for aggregation into one x8 port.

Hot Plug for High Availability

Hot plug capability allows users to replace hardware modules and perform maintenance without powering down the system. The ExpressLane PEX 8524 hot plug capabilities and advanced error reporting features make them suitable for High Availability (HA) applications. Each downstream port includes a Standard Hot Plug Controller. If the PEX 8524 is used in an application where one or more of its downstream ports connect to PCI Express slots, each port's Hot Plug Controller can be used to manage the hot-plug event of its associated slot. Furthermore, its upstream port is a hot-plug **client**, allowing it to be used on hot-pluggable adapter cards, backplanes and fabric modules.

Fully Compliant Power Management

For applications that require power management, the ExpressLane PEX 8524 device support both link (L0, L0s, L1, L2/L3 Ready, and L3) and device (D0 and D3hot) power management states, in compliance with the PCI Express power management specification.

SerDes Power and Signal Management

The ExpressLane PEX 8524 supports **software control** of the **SerDes outputs** to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical and high. The SerDes block also supports loop-back modes and advanced reporting of error conditions, which enables efficient debug and management of the entire system.

Flexible Virtual Channel Arbitration

The ExpressLane PEX 8524 switch supports hardware fixed and **Round Robin** arbitration schemes for two virtual channels. This allows fine tuning of Quality of Service, optimum use of buffers and efficient use of the system bandwidth.

Applications

Suitable for **host-centric** as well as **peer-to-peer** traffic patterns, the ExpressLane PEX 8524 can be configured for a wide variety of form factors and applications.

Host Centric Fan-out

The ExpressLane PEX 8524 device, with its versatile symmetric or asymmetric lane configuration capability, allows user specific tuning to a variety of host-centric applications.

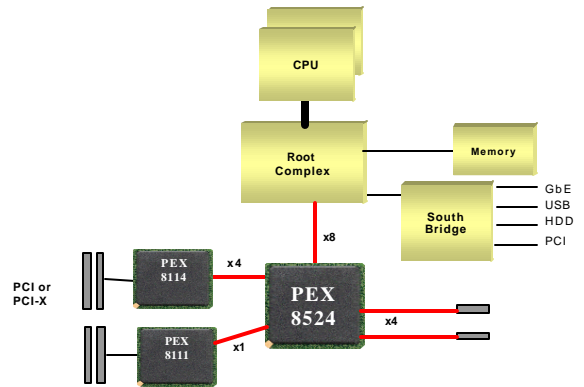


Figure 1. Fan-in/out Usage

Figure 1 shows a typical **server-based** design, where the root complex provides a PCI Express link that needs to be expanded into a larger number of smaller ports for a variety of I/O functions each with different bandwidth requirements.

In this example, the ExpressLane PEX 8524 would typically have an 8-lane upstream port, and as many as **5 downstream ports**. The downstream ports can be of differing widths if required. The figure also shows how some of the ports can be bridged to provide **PCI or PCI-X** through the use of the ExpressLane PCIe bridges such as **PEX 8114 and PEX 8111**.

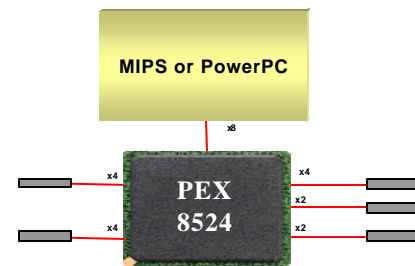


Figure 2. Fan out for PowerPC/MIPS CPUs

Almost all (non x86 based) high-end microprocessor manufacturers are offering PCI Express interfaces. PEX 8524 can be directly connected to a processor to fan-out its PCIe port to a larger number of ports for enhanced connectivity as illustrated in Figure 2.

Peer to Peer Communication

Figure 3 represents a backplane where the ExpressLane PEX 8524 provides peer-to-peer data exchange for a large number of line cards where the CPU/Host plays the management role.

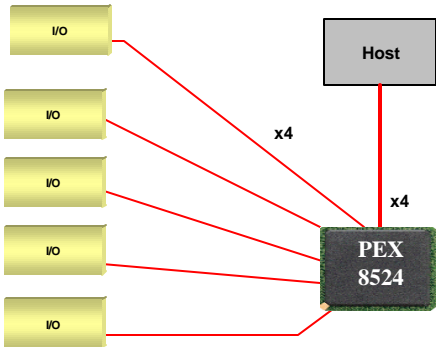


Figure 3. Peer to Peer Usage

Graphics Fan-out Switch

The number and variety of PCI Express native-mode devices is growing quickly. The devices such as PCIe graphics cards are expected to become mainstream very rapidly. As that happens, it will be necessary to take an x8 port on the root complex device and fan it out to two x4 (or x8) ports for dual graphics applications. Root Complex (Northbridge) devices are available with multiple PCIe ports. These ports can be further expanded to connect to a larger number of I/Os or to support dual-graphics using PEX 8524 as shown in Figure 4.

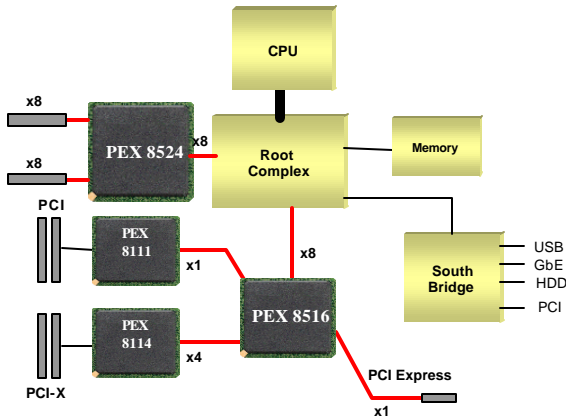


Figure 4. Graphics Fan-out

Intelligent Adapter Card

The ExpressLane PEX 8524 supports **non-transparency** bridging (NTB). Figure 5 illustrates a host system using an intelligent adapter card.

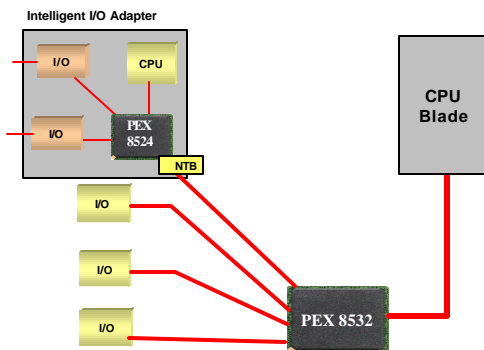


Figure 5. Intelligent Adapter Usage

In this figure, the CPU on the adapter card is isolated from the host CPU. The PEX 8524 non-transparent port allows the two CPUs to be isolated but communicate with each other through various registers that are designed in the PEX 8524 for that purpose. The host CPU can dynamically **re-assign** both the **upstream** port and the **non-transparent** port of PEX 8524 allowing the system to be reconfigured.

PCI Express Port Expansion

The PEX 8524 enables designers to take, for example, two x8 PCIe ports and expand them into ten ports. Some of these PCIe ports can be bridged to PCI or PCI-X using bridging products from PLX. Figure 6 illustrates one of the many configurations PEX 8524 can support.

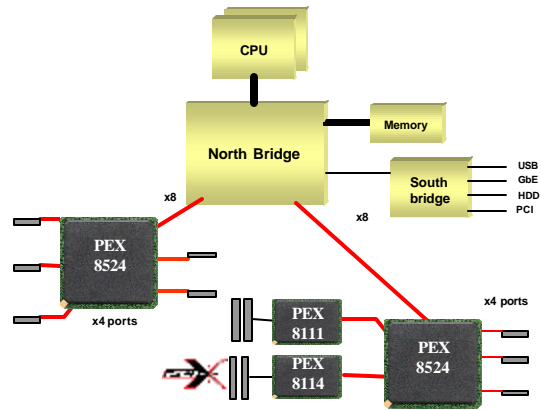


Figure 6. PCIe Port Expansion

Port Adapters

The number and variety of PCI Express native-mode devices is growing quickly. This will make it necessary to create multifunction and multi-port adapter cards with PCI Express capability.

The ExpressLane PEX 8524 can be used to create an adapter or mezzanine card that aggregates the PCI Express devices into a single port that can be plugged into a backplane or a motherboard. Figure 7 shows the PEX 8524 in this application.

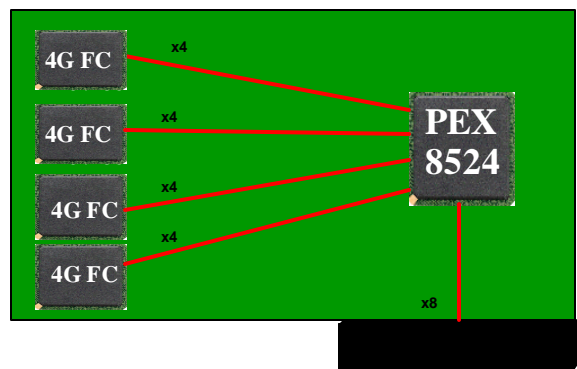


Figure 7. Adapter Cards

Software Usage Model

From a system model viewpoint, each PCI Express port is a virtual PCI to PCI bridge device and has its own set of PCI Express configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The virtual PCI to PCI bridges within the PEX 8524 are compliant to the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI to PCI bridge are accessible by type 0 configuration cycles through the virtual

primary bus interface (matching bus number, device number, and function number).

Interrupt Sources/Events

The ExpressLane PEX 8524 switch supports the INTx interrupt message type (compatible with PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by PEX 8524 for hot plug events, baseline error reporting, and advanced error reporting.

Development Tools

PLX is offering hardware and software tools (PEX 8524RDK) to enable rapid customer design activity. These tools are bundled in a Rapid Development Kit (RDK). The RDK consists of hardware, hardware documentation and Software Development Kit (SDK).

ExpressLane PEX 8524RDK

The RDK hardware module includes the PEX 8524 with one x8 (card-edge slot) port, two x4 ports and one x8 port. The RDK is available with x8 card edge connector/adaptor. The adapters for x4 and x1 edge connectors are available to plug the RDK in smaller slots.

The PEX 8524RDK board can be installed in a motherboard, used as a riser card, or configured as a bench-top board.

The PEX 8524RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for the PEX 8524 features and benefits.

PEX 8524RDK provide everything that a user needs to get their hardware and software development started.

SDK

The SDK tool set includes:

- Linux and Windows drivers
- C/C++ Source code, Objects, libraries
- User's Guides, Application examples, Tutorials

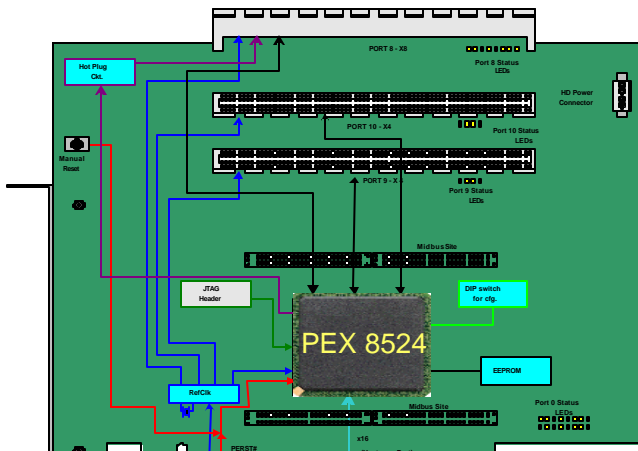


Figure 7. PEX 8524RDK

Product Ordering Information

Part Number	Description
PEX 8524-AA25VBES	24-Lane PCI Express Switch
PEX 8524VRDK-8	Rapid Development Kit for PEX 8524 (3 models)

Please visit the PLX Web site at <http://www.plxtech.com> or contact PLX sales at 408-774-9060 for sampling.



PLX Technology, Inc.
 870 Maude Ave.
 Sunnyvale, CA 94085 USA
 Tel: 1-800-759-3735
 Tel: 1-408-774-9060
 Fax: 1-408-774-2169
 Email: info@plxtech.com
 Web Site: www.plxtech.com

© 2004 PLX Technology, Inc. All rights reserved. PLX and the PLX logo are registered trademarks of PLX Technology, Inc. ExpressLane is a trademark of PLX Technology, Inc., which may be registered in some jurisdiction. All other product names that appear in this material are for identification purposes only and are acknowledged to be trademarks or registered trademarks of their respective companies. Information supplied by PLX is believed to be accurate and reliable, but PLX Technology, Inc. assumes no responsibility for any errors that may appear in this material. PLX Technology, Inc. reserves the right, without notice, to make changes in product design or specification.

PEX8524-SIL-PB-P.9