

# PEX 8524 BBV Migration Design Note

## Migrating from AAV to BBV Silicon Revision

### Purpose and Scope

Customers using the AAV silicon revision of the PEX 8524 (35mm x 35mm, 680-Ball PBGA package) device will be required to migrate to the BBV silicon revision as we are only going into full production with the BBV silicon revision. This document details any hardware and/or software considerations that need to be taken into account when migrating to the BBV silicon revision.

### 1 Background

The PEX 8524 is a first generation PCI Express switch from PLX Technology. It supports 24 PCI Express lanes that the user can configure in up to 6 ports. The PEX 8524 is currently only in production with the BBV silicon revision. Users of AAV silicon revision shall migrate to the BBV silicon revision.

### 2 Differences

The following sections describe the differences between the PEX 8524 AAV and BBV silicon revisions.

#### 2.1 Errata

With each silicon revision, certain errata were fixed. Table 1 shows which errata found in the AAV silicon revision have been fixed in the BBV silicon revision. The complete errata list with details on each erratum is available on the web at [www.plxtech.com](http://www.plxtech.com) in the PEX 8524 device toolbox. Be sure to download the latest file from the web for the most up-to-date errata list.

Table 1

Errata in rev. AAV silicon	Description	Risk Category	Fixed in rev. BBV silicon	Fix in PEX 8525 <sup>1</sup>
1.	NT: EEPROM Write	Low	No	N/A <sup>2</sup>
2.	Skip Ordered Sets During Training	Low	No	Yes
3.	Skew Causing Decode Issue	Low	No	Yes
4.	Fatal/Non-fatal Error Reporting Enable Retracted Erratum due to Redundancy – See Erratum #20	Low	No	Yes
5.	SerDes Reset Early in L1 State	Low	No	Yes
6.	Detect State Machine Active Early	Low	No	Yes
7.	NT: Register Shadowing	Low	No	N/A <sup>2</sup>
8.	Uncorrectable Error Log	Low	No	Yes
9.	Legacy INTx Mode: Interrupt Dropped	Medium	Yes	Yes
10.	De-skew Logic Out of Sync in L0s to L0 Transition	Low	No	Yes
11.	Need at Least Two TSI Ordered Sets	Low	No	Yes

Errata in rev. AAV silicon	Description	Risk Category	Fixed in rev. BBV silicon	Fix in PEX 8525 <sup>1</sup>
12.	FC Initialization	Low	Yes	Yes
13.	FC Initialization	Low	Yes	Yes
14.	NT: Non-zero BAR Enables	Low	No	N/A <sup>2</sup>
15.	VC1 Enable and Control Register	Low	No	Yes
16.	Secondary Bus Reset May Not Clear All Bits	Low	No	Yes
17.	x16 Mode Packet Corruption and Queue Flush	Medium	Yes	Yes
18.	NT: EEPROM Expansion ROM Access	Low	No	N/A <sup>2</sup>
19.	SERR Signaling	Low	No	Yes
20.	Fatal/non-fatal Error Message Generation	Low	No	Yes
21.	ISA/VGA Support	Medium	Yes	Yes
22.	Power Management Register Not Loaded Correctly	Low	No	Yes
23.	NT: Power Management Register Not Loaded Correctly	Low	No	N/A <sup>2</sup>
24.	Hot Reset Active Too Long	Low	No	Yes
25.	NT: Non-posted Transactions	Low	No	N/A <sup>2</sup>
26.	NT: Port CSR Clear	Low	No	N/A <sup>2</sup>
27.	False Rec Error While Transitioning from L0.Active to L0.L0s	Low	No	Yes
28.	NT: BAR3 Virtual Side Register	Low	Yes	N/A <sup>2</sup>
29.	BAR4 & BAR5 for 64bit Address in NTB Mode	Low	Yes	N/A <sup>2</sup>
30.	NT: Cardbus CIS Pointer	Low	No	N/A <sup>2</sup>
31.	Incorrect Address in MSI Interrupt Event	Medium	Yes	Yes
32.	Ordering Violation Under Extreme Credit Starvation	Medium	Yes	Yes
33.	JTAG-AC	Low	Yes	Yes
34.	Electrical_Idle Unpredictability	Medium	Yes	Yes
35.	Receiver_Detect Unpredictability	Medium	Yes	Yes
36.	Option to Reload EEPROM on Hot Reset Event Does Not Work	Medium	Yes	Yes
37.	64-bit BAR in NT Mode	Medium	Yes	N/A <sup>2</sup>
38.	64-bit BAR in NT Mode	Medium	Yes	N/A <sup>2</sup>
39.	Address Range in NT Mode	Medium	Yes	N/A <sup>2</sup>
40.	Increase the Core and SerDes Voltage	Medium	Yes	Yes
41.	Expansion ROM Limited to 2Kbyte	Low	Yes	N/A <sup>2</sup>
42.	Link Recovery from Link Down	Low	Yes	Yes
43.	BAR Setup Register in NT Mode	Low	Yes	N/A <sup>2</sup>

Errata in rev. AAV silicon	Description	Risk Category	Fixed in rev. BBV silicon	Fix in PEX 8525 <sup>1</sup>
44.	Having no EEPROM in NT Mode	Low	Yes	N/A <sup>2</sup>
45.	Wrong Manufacturers ID in the JTAG Registers	Low	Yes	Yes
46.	Increase the Core and SerDes Voltage to 1.15 V +- 3%	Medium	Yes	Yes
47.	Unreliable Power Up BIST Status	Low	Yes	Yes
48.	EEPROM Reload Side Effects	Low	No	Yes
49.	NT: LUT Entry Write Corrupts Setup Register	Low	No	N/A <sup>2</sup>
50.	Receiver Error Status Stuck on De-Skew Overflow Event	Low	No	Yes
51.	Non-existent Device Read Request Could Cause Credit Leak when Interspersed with Posted Traffic	Low	Yes	Yes
52.	Disabling Memory or I/O-Upper Base & Limit Range	Low	Yes	Yes
53.	Rejected Transactions when 64-bit Space is Below 4G	Low	Yes	Yes
54.	Rejected Transactions when Downstream Port in D3hot State	Low	Yes	Yes
55.	AC-JTAG Not Supported	Low	No	No

Notes:

1. The PEX 8525 is a 24 lane switch based on PLX's 3<sup>rd</sup> generation architecture supporting added features and enhanced performance. The PEX 8525 is pin-compatible to the PEX 8524. A migration document with guidelines on how to migrate your PEX 8524 design to the PEX 8525 is available. Please contact your local Sales Rep. for more information on the PEX 8525. PEX 8525 General Samples will be available in Q4 2006.
2. The Non-Transparent (NT) functionality does not exist in the PEX 8533, and therefore this erratum is not applicable.

## 2.2 Power Requirements

The SerDes and Core VDD Max Voltage and Max Power Dissipation differ between the AAV and BBV silicon revisions (see Table 2). Customers migrating to the BBV silicon revision from the AAV silicon revision will need to adjust their power supply to be in accordance with the electrical specifications for the BBV silicon revision (1.0V ± 5%). Not doing so may lead to device and/or system failure. Complete electrical specifications can be found in the Data Book which is available at [www.plxtech.com](http://www.plxtech.com) in the PEX 8524 device toolbox.

Table 2

PEX 8524 Silicon Revision	SerDes & Core VDD Max Voltage (V)	Max Power Dissipation (W)
AAV	1.15 ± 3%	9.08
BBV	1.0 ± 5%	7.38

## 2.3 Thermal Characteristics

The BBV silicon revision is offered in Industrial Temperature grade whereas the AAV silicon revision is only offered in Commercial Temperature grade. Please refer to Table 3 below for differences in operating temperature ranges as well as heat sink and airflow requirements. Complete thermal specifications can be found in the Data Book which is available at [www.plxtech.com](http://www.plxtech.com) in the PEX 8524 device toolbox.

Table 3

PEX 8524 Silicon Revision	Commercial Temperature			Industrial Temperature		
	Operating Temp. (°C)	Heat Sink Required	Airflow Requirement	Operating Temp. (°C)	Heat Sink Required	Airflow Requirement
AAV	0 to +70°	Yes	2 m/s	N/A	N/A	N/A
BBV	0 to +70°	Yes	1 m/s	-40 to +85°	Yes	2 m/s

## 2.4 EEPROM

For customers using an EEPROM with their design, the EEPROM image will need to be updated whenever the silicon revision is changed. Below is a list of EEPROM changes that will apply to AAV to BBV migrations.

### EEPROM Changes for AAV to BBV Migrations

1. In all ports (Ports 0-3, 8-11, NT-Virtual and NT-Link), change the Revision ID (offset 08h) value from AAh to BBh, so that the software can correctly identify the silicon revision.
2. In Port 0 offset 1DCh, remove the Errata #36 (EEPROM Load on Hot Reset) workaround, since this revision AAV erratum is fixed in revision BBV, and EEPROM reload on either a Hot Reset or upstream port link down condition should normally be enabled.
  - a. Clear the Hot Reset EEPROM Load Disable, bit 17 (default value 0). This bit is set (1) for revision AAV particularly if not all ports are enabled (i.e., if Ports 0 and/or 8 offset 224h values are not zero).
  - b. In Transparent Mode designs (Port 0 offset 1DCh bits [19:18] = 11b), clear the Hot Reset Propagation Disable, bit 20 (default value 0), since a Hot Reset to the upstream port or an upstream port link down condition should normally allow both soft reset of the PEX 8524 and issuance of a Hot Reset to downstream devices.
3. In all transparent ports (Ports 0-3, 8-11) offset 1E0h, enable Link Retrain on DLLP Timeout by clearing bit 8 to its default value 0, to allow faster detection and recovery if a port's link goes down. Bit value definition is inverted from revision AAV to revision BBV; default value (0) is unchanged. Link Retrain on DLLP Timeout is always enabled for the NT port.
4. In Ports 0 & 8 offset 220h, disable InitFC Triplet Mode by setting bit 7 to its default value 1, since Triplet mode should not be enabled due to an erratum that could prevent linkup. Bit value definition is inverted from revision AAV to revision BBV; default value (1) is unchanged.
5. Clear Ports 0 & 8 offset 22Ch, unless Never Detect Electrical Idle (bit 4) and/or Always Detect a Receiver (bit 0) must be set for interface to particular devices (note that link width negotiation to a narrower than programmed port width is disabled if bit 0 is set). The Never Detect Electrical Idle bit needed to be set in revision AAV for Errata #34, which is fixed in revision BBV, and electrical idle detection is needed for certain LTSSM transitions such as enabling the device at the other end of the link to transition to its L0s state. Also, clearing bit 1 in offset 22Ch enables the K28.5 Framer Filter,

which increases the robustness of the framer logic by not retraining the link until four consecutive COM symbols are received, instead of retraining the link after a single COM symbol is received; bit value definition is inverted from revisions AAV to revision BBV; default value (0) is unchanged.

For further guidance on programming the EEPROM, customers may refer to the EEPROM Design Note, which is available at [www.plxtech.com](http://www.plxtech.com) in the PEX 8524 device toolbox.

## 2.5 Registers

The following changes to the register configurations are required when migrating to the BBV silicon revision.

1. PEX 8524 revision BBV default Device ID (offset 00h[31:16] in all ports) value is changed from 8532h to 8524h.
2. Revision BBV NT-Link port Expansion ROM register (offset 30h) enables 32KB of memory space in place of 2KB enabled by revision AAV (bits [14:11]).
3. Revision BBV transparent ports (0-3 and 8-11) add support for legacy VGA by supporting the VGA Enable bit (offset 3Ch[19]) and the ISA Enable bit (offset 3Ch[18]).
4. Revision BBV transparent ports (0-3 and 8-11) add support for the VGA 16-Bit Decode bit (offset 3Ch[20]), to update PCI-to-PCI Bridge Architecture Specification compliancy from v1.1 to v1.2.
5. Revision BBV changed the default value of the Prefetchable Base Upper 32-bits [63:32] registers (offset 28h in Ports 0-3 and 8-11), from FFFFFFFFh to 0h. The default values of the corresponding AMCAM (Address-Mapping CAM) Registers in Ports 0 & 8 offsets 350h, 360h, 370h, 380h, 3D0h, 3E0h, 3F0h and 400h are also changed from FFFFFFFFh to 0h.
6. Revision BBV changed Ingress Credit Handler (INCH) Threshold register default values for VC0, in Ports 0 & 8 registers A00h - A04h, A18h - A20h, A30h - A38h, and A48h - A50h. The new values provide increased performance over revision AAV when no EEPROM is present.
7. Revision BBV adds the PLX-Specific Relaxed Completion Ordering feature that can be enabled in Ports 0 & 8 offsets BECh[0] and BFCh.

## 3 Compatibility

The following sections describe the compatibilities between the PEX 8524 AAV and BBV silicon revisions. Please note that device functionality will remain unchanged in the BBV silicon revision.

### 3.1 Package

Both silicon revisions (AAV and BBV) are packaged in a 35mm x 35mm, 680-Ball PBGA package and are fully compatible in package dimensions, ball spacing (pitch), and ball sizes. PCB pad dimensions need not be altered.

### 3.2 SerDes Locations

All 24 PCI Express SerDes LVDS pairs' (lanes) locations and polarity between both silicon revisions (AAV and BBV) are identical.

### 3.3 Strapping Signals

Both silicon revisions (AAV and BBV) provide the same five strapping pins (signals) to configure the ports on Station 0 and four strapping pins (signals) to configure the ports on Station 1.

### 3.4 Power Pins

Power and Ground pins are in the exact same locations on both silicon revisions (AAV and BBV).

### **3.5 Lane Good Signals**

Both silicon revisions (AAV and BBV) support one PEX\_LANE\_GOOD# signal for each lane, allowing designers to connect them to LEDs to show the link-up status of each lane.

### **3.6 Registers**

All registers not mentioned in section 2.5 will remain unchanged in the BBV silicon revision.