

2.4GHz wireless audio streamer

nRF24Z1

FEATURES

- Single chip low cost 0.18u CMOS, 36 pin 6x6mm QFN package
- Single chip 2.4GHz RF transceiver
- 4Mbit/sec RF link
- Input sample rate up to 96kHz, 24bits
- Output sample rate up to 48kHz, 16bits
- Programmable latency
- Quality of Service engine supporting up to 1.536 Mbit/s LPCM audio
- S/PDIF interface for direct connection to PC soundcard and surround receivers
- I2S interface for glueless audio support
- SPI or 2-wire interface for up to 12 kbit/sec peak bi-directional digital control/AUX data
- On chip optional 2:1 compression
- On chip voltage regulators
- Few external components
- Uses global 2.4GHz band

APPLICATIONS

- Compact Disk, CD quality headset
- MP3 / Mini Disk headset
- Speakers
- Surround speakers
- Microphone
- Musical instruments
- Audio streaming from PC soundcard to HiFi system
- Download MP3 files from PC to MP3 player
- Compressed video streaming

GENERAL DESCRIPTION

nRF24Z1 gives you a true single chip system for CD quality audio streaming of up to 16 bit 48 kHz audio with support of up to 24 bit 96 kHz input. I2S and S/PDIF interfaces are supported for audio I/O. Seamless interfacing of low cost A/D and D/A for analog audio input and output. SPI or 2-wire (I2C compatible) serial interfaces for control. The circuit has embedded voltage regulators, giving maximum noise immunity and operation from a single 2.0V to 3.6V supply.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	2.0	V
Temperature range	-20 to +80	°C
Peak supply current in transmit @ -5dBm output power	15	mA
Peak supply current in receive mode	32	mA
Supply current in power down mode	3	µA
Maximum transmit output power	0	dBm
Audio sample rate	8, 16, 32, 44.1 or 48	kbps
Audio resolution	16	bit
Receiver sensitivity	-80	dBm

Table 1-1 nRF24Z1 quick reference data.



ORDERING INFORMATION

Type number	Description	Version
nRF24Z1-ES	36L QFN 6x6 mm	A
nRF24Z1-EvKit	Evaluation kit	1.0

Table 1-2 nRF24Z1 ordering information.



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1 ARCHITECTURAL OVERVIEW

nRF24Z1 is a 4 MBit/s single chip RF transceiver that operates in the world wide 2.4 GHz ISM band. The nRF24Z1 is based on the proven nRF24xx radio and ShockBurst platforms from Nordic Semiconductor.

The device offers a wireless channel for seamless streaming of LPCM or compressed audio in parallel with a low data rate control channel. To enable this, the device offers the following features in addition to the nRF24xx RF platform:

- Standard digital audio interfaces (I2S, S/PDIF)
- Fully embedded Quality of Service engine that handles all RF protocol and RF link tasks.
- SPI and 2-wire master and slave control interfaces
- GPIO pins

As all processing related to audio I/O, RF protocol and RF link management is embedded, the device offers the end application an up to 1.54 MBit/s transparent audio channel without any true time processing needed. nRF24Z1 can be utilized in systems without external microcontroller or by a simple microcontroller that only need to handle low speed tasks over the serial or parallel ports (ex: volume up/down).

A typical system using nRF24Z1 can be seen in Figure 1-1

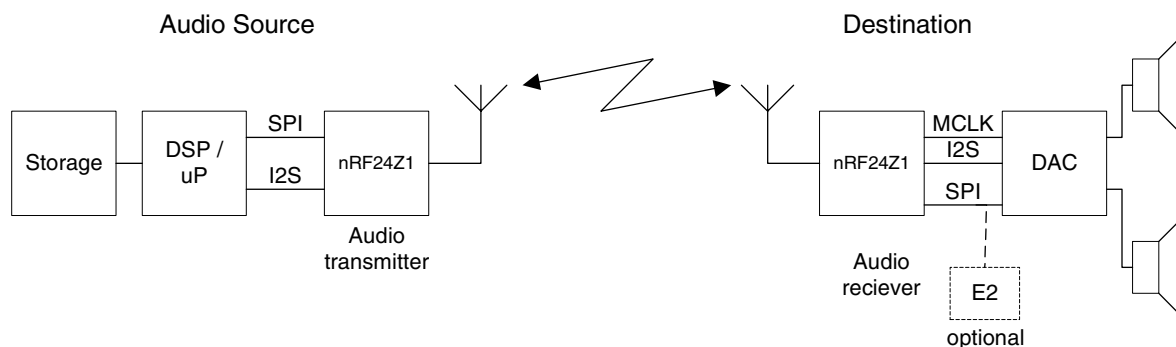


Figure 1-1 Typical audio application using nRF24Z1

In this system a DSP or micro controller feeds data from storage to nRF24Z1 using standard audio format (I2S). A nRF24Z1 pair transfers the audio data and presents it to a stereo DAC on the other side. For other parts of the application, the nRF24Z1 link will in other words look like an open channel (like a cable).

Initial configuration of nRF24Z1 is done by the micro controller, if present, through a SPI or 2-wire control interface. On the destination side, peripherals like a DAC can be controlled from the audio source side through the control channel offered by nRF24Z1.

In designs without an external micro controller, configuration data can be loaded by nRF24Z1 from an optional EEPROM/FLASH memory.



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A wireless system that is streaming audio will have a very asymmetrical load on the RF link since audio data is fed from an audio source (CD player) to a destination (loud speakers). From the destination back to the audio source only service and control communication is needed.

The nRF24Z1 are used both on the audio source side (ex. in a CD player) transmitting audio data, and in the 'destination' (loud speaker) side receiving audio data. Due to the asymmetry, nRF24Z1 has two main modes set by external pin TXSEL, depending on which side of the link it is put. The two modes have significant differences both in internal and I/O functionality.

To ease understanding of nRF24Z1 operation, the following notation is introduced:

- ATX, Audio transmitter – nRF24Z1 on the audio source side, transmitting audio data
- ARX, Audio receiver – nRF24Z1 on the destination side, receiving audio data

Transmitter and receiver are here referring to the flow of the audio; the nRF24Z1 RF front end always runs a full two way link.

The control channel is a two way low data rate channel superimposed on the audio and service communication. The audio transmitter is designated master meaning that when a RF link is present 2-wire, SPI, GPIO and internal registers in the audio receiver can be seen and controlled as a virtual extension of the audio transmitters own I/O and registers.

The implications of this is that external devices like audio DAC or volume control components connected to the audio receiver effectively is controlled by input to the audio transmitter. User actions (ex: push of a button) on the audio receiver side are similarly fed back to and can be processed on the audio transmitter side.

The following sections will give an overview of the functionality, I/O and main modules of nRF24Z1. Due to the significant differences in ATX and ARX, the overview will present the modes separately.



1.1 Audio transmitter

When nRF24Z1 is put at the audio source side of the RF link, TXSEL must be clamped high and nRF24Z1 becomes an audio transmitter (ATX). The block schematic of nRF24Z1 in ATX mode can be seen in Figure 1-2.

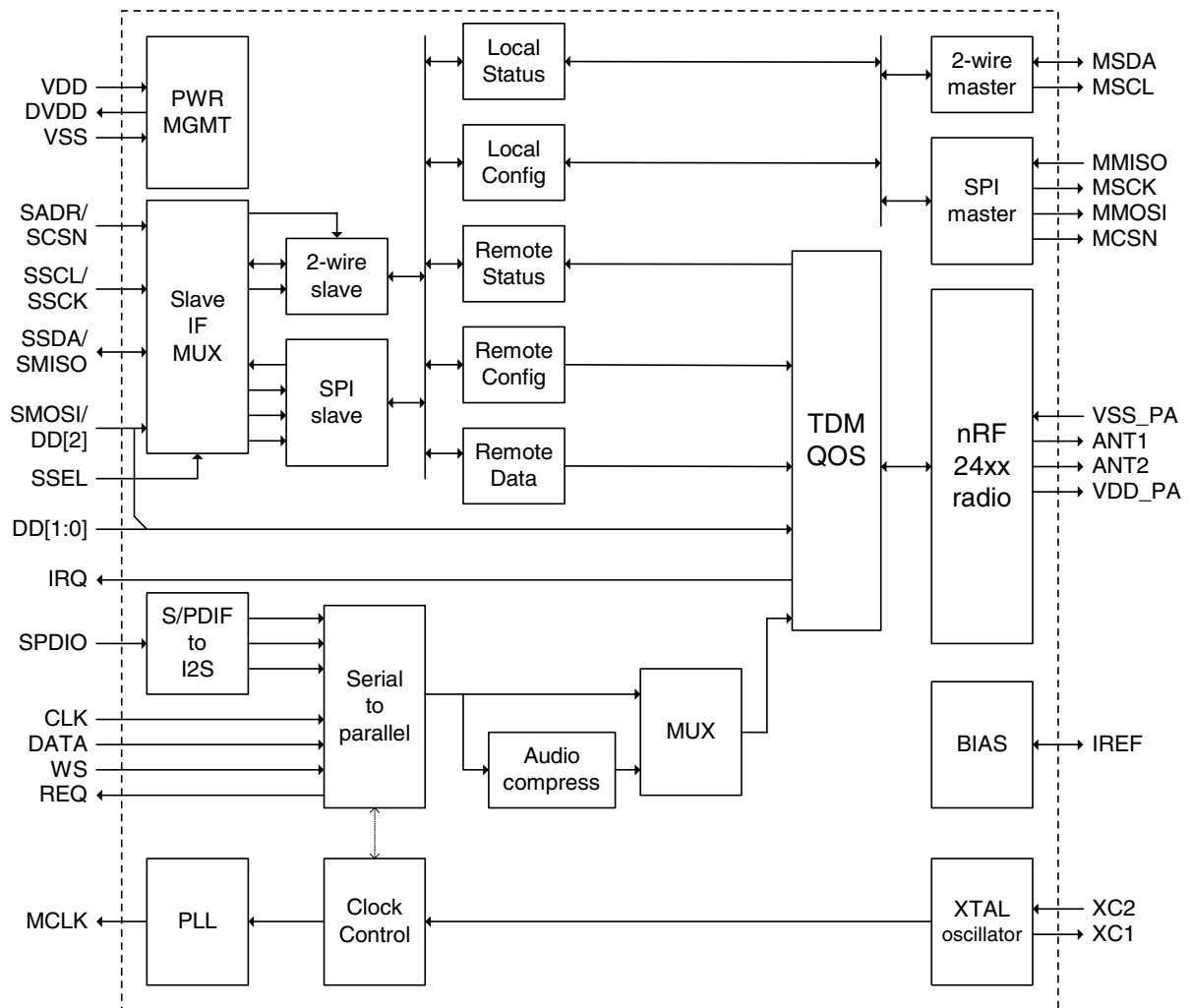


Figure 1-2 nRF24Z1 ATX mode block diagram

The I2S or S/PDIF can be used for audio data input or alternatively the device may stream other real-time data from a DSP over the I2S interface.

If ATX is controlled by an external MCU, configuration and control data, both for the audio transmitter and for a connected audio receiver may be entered via the 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical for both interfaces, but only one of the interfaces, selected by SSEL pin, may be used in a given application.

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For stand alone operation of nRF24Z1, a serial EEPROM or FLASH memory may be connected to the SPI or 2-wire master interface. If a memory is present at any of these interfaces during power up, the device will read default configuration data from the memory.

1.1.1 I2S audio input

For seamless input from audio sources physically close to nRF24Z1, the single end I2S is the preferred interface. The interface supports sample rates of 8, 16, 32, 44.1, 48 and 96 kHz. Data may be in 16, 20 or 24 bit format.¹

I2S may also be used with an external stereo ADC for analog audio sources. The ADC may be clocked at 256 times f_s by the MCLK output from nRF24Z1.

A REQ output is available for pacing the data-flow when streaming MP3 or other “data” streams over the I2S.

1.1.2 S/PDIF audio input

For physically more remote audio sources the audio transmitter provides (single ended CMOS) S/PDIF input. This interface supports 32, 44.1 or 48 kHz and 16, 20 or 24 bit data. The data rate is automatically detected.

1.1.3 Control (slave) interfaces

nRF24Z1 has 2 alternative slave interfaces available for microprocessor control of the operation. The pin SSEL selects the interface:

SSEL = 0; SPI (pins SCSN, SSCK, SMISO, SMOSI).

SSEL = 1; 2-wire (pins SADR, SSCL and SSSDA)

1.1.3.1 SPI slave interface

The SPI slave can operate with up to 8 MHz clock speed over the full operation range of the device. With a 3V +/-10% supply the maximum clock speed is 16MHz.

1.1.3.2 2-wire slave interface

This interface is primarily intended for applications where the audio transmitter is controlled by a low-end microprocessor. The interface is similar to what is found on serial memories and data converter devices. The interface supports 100 kHz, 400 kHz and 1MHz over the operating range of the device. The 7-bit device address of nRF24Z1 is ‘a101001’, where ‘a’ is the logic level of the SADR input pin (read during power up and reset only).

1.1.4 Master interfaces

nRF24Z1 offers 2 alternative master interfaces primarily intended for connection to external memory when nRF24Z1 is to be operated without external micro processor.

1.1.4.1 SPI master interface

In the audio transmitter the SPI master is operated at 1MHz or 0.5MHz. SPI format is CPOL=0,CHPA=0 as used by industry standard EEPROM/FLASH memories.

¹ This specification item specifies the interface. Not all of these formats can be transferred within the available 1.54 Mbit/s data rate.


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1.1.4.2 2-wire master interface

In the audio transmitter this interface is operated at 100 kHz for compatibility with virtually all serial 2-wire memories.

1.1.5 Direct data input pins

The audio transmitter has 2 pins DD[1:0] that may be transmitted directly to the audio receiver. When SSEL is set high (2-wire interface selected), one additional direct data pin (DD[2]) is available. The logic level on pins DD[2:0] will be copied over the control link to the audio receiver pins DO[2:0]. These pins may be used to switch on/off audio receiver peripherals without microprocessor activity.

1.2 Audio Receiver

When nRF24Z1 is put at the destination side of the RF link, TXSEL must be clamped low and nRF24Z1 becomes the audio receiver (ARX). The block schematic of nRF24Z1 in ARX mode can be seen in Figure 1-3

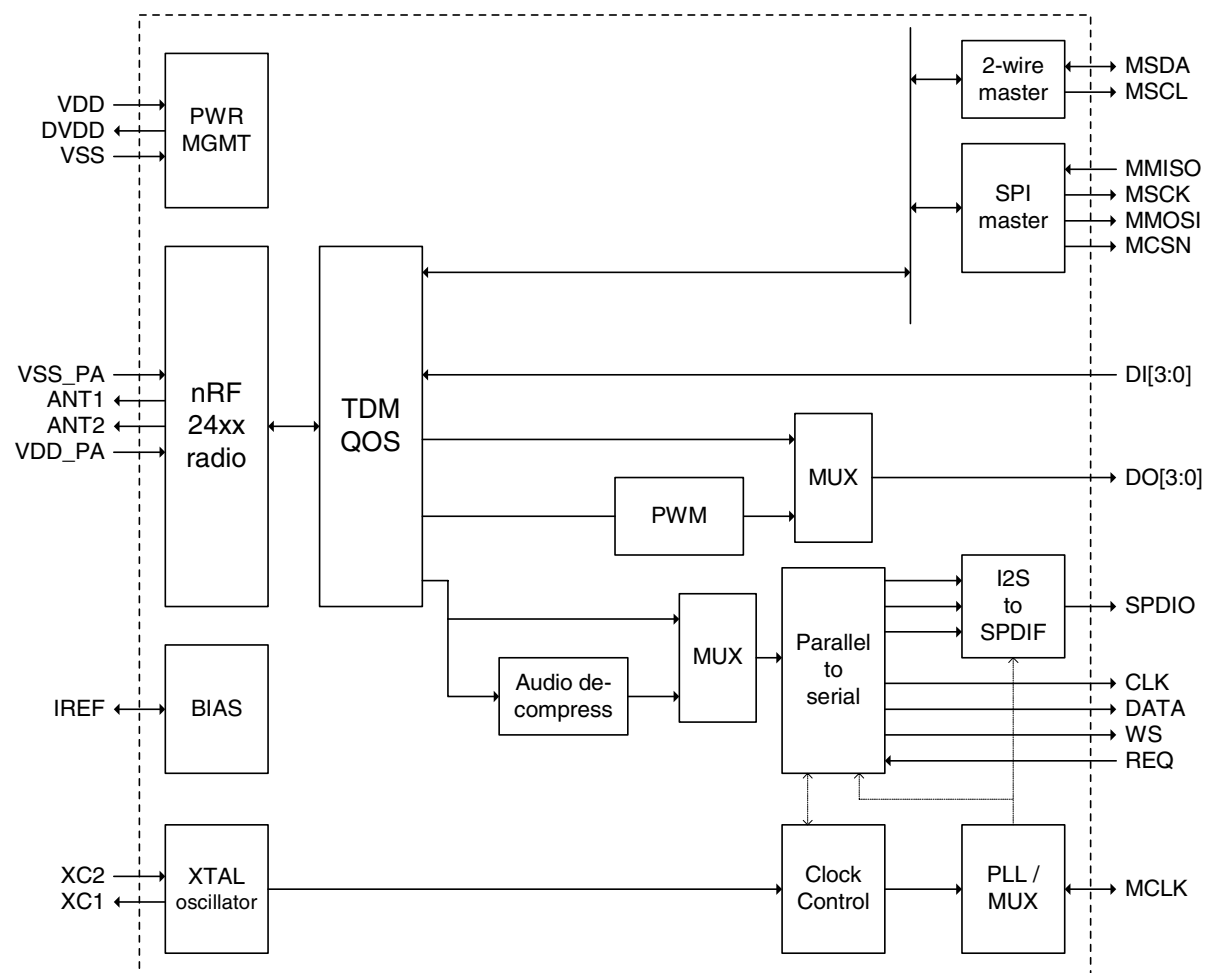


Figure 1-3 nRF24Z1 ARX mode block diagram



I2S or S/PDIF are used for audio or other real time data output.

A serial EEPROM or FLASH memory may be connected to the SPI or 2-wire master interface. If a memory is present at any of these interfaces during power up, the device will read default configuration data from that memory, otherwise hardcoded default values will be used.

After a link is established the user can control the SPI and 2 wire master from the audio transmitter. In this way the audio transmitter is able to control audio receiver serial peripherals like audio DACs and amplifiers.

1.2.1 I2S audio output

Audio output to devices physically close to nRF24Z1 (typically a stereo DAC) are normally driven by the I2S output. The interface supports sample rates of 8, 16, 32, 44.1 and 48 kHz. Data may be in 16 or 24 bit format.

In audio receiver mode the MCLK pin is output. It can be configured to provide 256 times f_s clock to an external DAC.

A REQ input is available for pacing the data-flow when streaming MP3 or other “data” streams over the I2S.

1.2.2 S/PDIF audio output

For physically more remote audio devices, the audio receiver provides an S/PDIF (full swing CMOS) output. This interface supports 32, 44.1 and 48 kHz, 16 or 24 bit data.

1.2.3 SPI master interface

During audio receiver start-up, the SPI master is operated at 1MHz or 0.5MHz with the SPI format set to CPOL=0,CHPA=0 for EEPROM/FLASH compatibility. After a link is established, the user may program the speed and format of the SPI master from the audio transmitter. The available clock speed is up to 8 MHz over the full operation range of the device.

1.2.4 2-wire master interface

During start-up, the audio receiver operates this interface at 100 kHz. After a link is established, the user may program the speed of the SPI master from the audio transmitter to 100kHz, 400kHz or 1MHz.

1.2.5 Parallel port and PWM

An 8 bit parallel port can be controlled and read from the audio transmitter. There are 4 input pins that are continuously monitored when a link is up. Changes on any of these inputs will be sent back to the audio transmitter where it can be accessed in a register (on the 2-wire/SPI bus). The audio receiver can be programmed to wake up from power down mode on a change on one of these pins.

There are 4 outputs DO[3:0] that are controlled from the audio transmitter. Any of these may be programmed for high current in order to drive LEDs or for standard CMOS to control of other devices on the audio receiver board.

DO3 may be programmed to output a PWM signal, where the output duty cycle is programmable with 8-bit resolution from the audio transmitter.



1.3 Blocks common to audio transmitter and receiver

1.3.1 XTAL Oscillator

The crystal oscillator will provide a stable reference frequency with low phase noise for the radio and audio functions. See ch. 5.3 for Crystal Specification.

1.3.2 Radio Transceiver

The transceiver part of the circuit is a member of nRF24xx family of low power highly integrated 2.4GHz ShockBurst™ transceivers. The transceiver interface is optimized for high speed streaming of up to 4 Mbps. Output power and channel selection can be controlled by the user via the QoS module.

1.3.3 Quality of Service and Time Division Multiplex module

The primary function is to deliver robust communication channel between the audio transmitter and audio receiver in an audio streaming application. Several data streams with different properties are handled. The available bandwidth is shared between audio data, service data and remote data. Data integrity is controlled by handshaking and packet retransmission. A secondary function of the QoS module is to initiate the connection between a audio receiver and its intended audio transmitter. Several schemes are available to enable the connection to be established without end user involvement.

On the audio transmitter, a programmable IRQ line is available for the QoS to get the attention of an external micro-controller if available. The IRQ can be set (active high or low) on requested data received on the link, audio receiver GPIO changes, packet loss exceeding programmable limit or broken link.

1.3.4 Audio compression / Decompression

A low delay (less than 1ms) audio compression algorithm is included. This function can be enabled by the user to conserve power by reducing the required transmit/receive times or to increase the dynamic range with a constant signal to noise ratio for 24-bit input signals.

1.3.5 Power management

nRF24Z1 can be put into several low power modes under user control. The audio transmitter power modes are controlled directly via SPI or 2-wire interface, whereas the audio receiver power modes are controlled over the link. The different power down modes enables the user to trade between current consumption and wakeup time. In deep power down the current consumption is typically 3µA, with a startup time of a few milliseconds. The audio receiver device can exit the power down modes by an external pin event on any of the DI pins or by a programmable wakeup timer. When a audio receiver wakes up it will try to establish a link as described in paragraph 2.2. The audio receiver may be configured to automatically return to power down mode after a programmable time if no link is established.



2 OPERATION OVERVIEW

2.1 Power up sequence

When supply is applied nRF24Z1 goes into power on reset. During reset all bi-directional pins are tri-stated to avoid driving conflicts and default content is set in all registers. The reset is held until supply voltage is kept above minimum supply voltage for a few milliseconds.

When power on reset is finished the device should be configured. There are 3 ways nRF24Z1 can be configured:

1. After power on reset nRF24Z1 will look for an external EEPROM/FLASH memory on the SPI master interface, if such a memory is present, configuration data is loaded, which means that all registers values are read from the external memory. If no memory is present on the SPI master interface, the procedure is repeated on the 2-wire master interface. These data will override the default content of nRF24Z1 registers.
2. An external micro processor configures nRF24Z1 through slave SPI or 2-wire serial interface, by writing to any of the configuration registers.
3. If no external memory is present and no configuration is done from an external MCU nRF24Z1 will start the link initialization with the default register content.

nRF24Z1 will then start a link initialization procedure based on the link configuration data. The value of the TXSEL pin determines whether it will be in ATX or ARX mode.

2.2 Link initialization

The link channel configuration registers, CHP1, CHP2, CHP3 determine the frequency hopping scheme of the nRF24Z1 radio transceiver. These registers have initial values which are common to all nRF24Z1 chips. After power on reset nRF24Z1 will look for an external EEPROM/FLASH as described above, and in case new values for CHP1, CHP2, CHP3 will override the initial values. After that an nRF24Z1 audio transmitter will start transmitting on radio channels according to the frequency hopping scheme derived from the CHP1, CHP2, CHP3 registers. In the same way a nRF24Z1 audio receiver will start receiving on radio channels according to a frequency hopping scheme derived from its CHP1, CHP2, CHP3 registers. To be able to establish a link, the content of the CHP1, CHP2, CHP3 register must be identical, implying identical frequency hopping schemes.

A nRF24Z1 audio transmitter will hop to a new channel in its scheme each TBD ms. A nRF24Z1 audio receiver will hop to a new channel in its scheme at a longer interval TBD ms, until it is able to receive something, then it will send an acknowledge packet, and from there on use the same frequency hopping interval as the audio transmitter.

By writing new values to CHP1, CHP2, CHP3 registers, the user can change the frequency hopping scheme. By turning ATX off and on (TXMOD register bit 7) ARX will loose link, and will use the new values trying to establish a new link.



2.3 Audio streaming

As long as a link is available, audio fed into the audio transmitter will be reproduced on the audio receiver. The total delay from input (I2S / S/PDIF) to output (I2S / S/PDIF) is programmable to be 5 ms, 10 ms or TBD ms. Data integrity is controlled by retransmitting packets that the audio receiver did not get or got with corruption, and by the slow frequency hopping algorithm. If transmission quality is too poor, packets may be lost even after retransmit. The user can read out the packet loss statistics from a register at the audio transmitter and use this to visualize the quality of the link. nRF24Z1 may be programmed to give an IRQ pulse if the rate of packet loss supersedes a programmable level, if an audio packet is permanently lost or if link is broken (a certain number of unsuccessful attempts to transmit data).

2.3.1 Audio receiver clock rate recovery

The audio transmitter will derive a low frequency (< 2kHz) rate signal by integrating the sample (word) clock in case of PCM transmission. For data (for example compressed audio), the same rate signal is derived by division of the clock signal from the XTAL oscillator. The low frequency rate signal is embedded in the RF packets during transmission to the audio receiver.

The audio receiver derives an output rate signal with nominally the same frequency by division of the MCLK ($256 \times F_s$) clock generated locally. The rate signal received embedded in the RF stream and the locally generated rate signal are both feed to a digital PLL that is in turn used to control the exact MCLK frequency. The digital PLL provides discrete output frequencies with a resolution of better than 25ppm. The bandwidth of the digital PLL is very low. To get close to the correct frequency, the filter is initialized during the initial 2 to 10 ms while the system buffers are filled.

For audio (PCM) transmission, this scheme will effectively create a audio receiver MCLK locked to the audio source (I2S or S/PDIF) on the audio transmitter. The PLL will lock for any input rate +/- 500 ppm off its nominal sample rate. The clock jitter is 250 ps RMS over the audio bandwidth, making it suitable for low cost DAC solutions.

For data transmission, the MCLK is effectively locked to the audio transmitter crystal oscillator. The clock division ratios are set up such that the MCLK frequency will be suitable for use in a DAC after an eventual decoder. The average rate of data should match the value written to the I2SRAT register on the transmit rate, but instantaneous rate may be up to 4 times as high.

2.4 Data link

There is a 2-way, low bit rate, robust data link running in parallel with the audio stream. The data link enables the audio transmitter to perform IO transfer the audio receiver (both GPIO, 2-wire and SPI with up to 4 slave devices).

2.5 Power saving modes

nRF24Z1 has 2 different power saving modes called “Standby” and “Powerdown”. The mode to use will depend on requirements for power consumption and startup time. Within each mode, the user can trade current consumption and startup time by adjusting the timer values in nRF24Z1 registers.



2.5.1 Standby mode

Standby mode is a link parameter affecting both audio transmitter and audio receiver. In this mode, nRF24Z1 devices maintain a radio link. Current is saved by the fact that only very short RF packets are transmitted, and in between the packets each device may enter a low power “idle” state (consuming less than 50 μ A). Both ARX and ATX will wake up at a programmable interval, look for a resume condition and interchange one short packet in each direction. The ATX is responsible for leaving the Standby mode (by clearing the standby bit in the register interface), however since the four DI3,DI2,DI1,DI0 signals are transmitted from ARX to ATX in the short data packet, the user may implement a startup initiated from the ARX side by connecting a “push button” or a microcontroller to any of the DI pins and programming nRF24Z1 appropriately.

2.5.2 Powerdown mode

In this mode, the radio link is shut down. The ARX device will enter a “stop” state (consumption 2-3 μ A). In the “stop” state, only a slow RC timer is operating. The ARX will wake up from the “stop” state at a regular interval and/or on a change on any of the four DI3,DI2,DI1,DI0 pins. When the ARX part wakes up, it will try to establish a link as described in 2.2 above. Typically the ARX device will be program to attempt to establish a link for a certain period of time. The average current consumption will be determined by the time spent looking for a link partner (using some mA) compared to the time in “stop” mode. Minimum current consumption in a portable ARX is achieved when the ARX is only programmed for wakeup on DI pin events.

The ATX device may also be put in “stop” state during Powerdown, with a programmed wakeup interval. Each time the ATX then wakes up, it will try to establish a link as described in 2.2 above. The average current consumption will be determined by the time spent looking for a link partner (using some mA) compared to the time in “stop” mode.



3 DETAILED DEVICE DESCRIPTION

This section describes in more detail all registers available to the user to influence the operation of nRF24Z1, to acquire information from the audio receiver or from the quality of service module. The register addresses in this section is the 7-bit address part of the command byte if registers are accessed over the SPI bus. For access to the registers over the 2-wire bus, the 7-bit address is found in the sub-address byte transmitted immediately after the device address.

3.1 Audio transmitter configuration registers

The registers described in this section control nRF24Z1 when acting as a audio transmitter. The power on reset values should be adequate to get a simple link up and running, but more sophisticated systems will require that these values are updated, either from a serial EEPROM read during power up, or more commonly from a CPU over one of the 2 serial control interfaces.

Address Hex	Register	R/W	Initial Hex	Description																																		
0x01	TXSTA	R	0x40	Audio transmitter status register																																		
				<table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Reserved, do not use</td> </tr> <tr> <td>6:5</td> <td>Detected audio scale factor (I2S only)</td> </tr> <tr> <td></td> <td> <table border="1"> <thead> <tr> <th>Value (bin)</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0.25</td> </tr> <tr> <td>01</td> <td>0.5</td> </tr> <tr> <td>10</td> <td>1</td> </tr> <tr> <td>11</td> <td>2²</td> </tr> </tbody> </table> </td> </tr> <tr> <td>4:3</td> <td>Detected audio fundamental rate</td> </tr> <tr> <td></td> <td> <table border="1"> <thead> <tr> <th>Value (bin)</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>48 kHz</td> </tr> <tr> <td>01</td> <td>44.1 kHz</td> </tr> <tr> <td>10</td> <td>32 kHz</td> </tr> <tr> <td>11</td> <td>Illegal or no input detected</td> </tr> </tbody> </table> </td> </tr> <tr> <td>2:0</td> <td>Audio transmitter state (TBD)</td> </tr> </tbody> </table>	Bit	Interpretation	7	Reserved, do not use	6:5	Detected audio scale factor (I2S only)		<table border="1"> <thead> <tr> <th>Value (bin)</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0.25</td> </tr> <tr> <td>01</td> <td>0.5</td> </tr> <tr> <td>10</td> <td>1</td> </tr> <tr> <td>11</td> <td>2²</td> </tr> </tbody> </table>	Value (bin)	Interpretation	00	0.25	01	0.5	10	1	11	2 ²	4:3	Detected audio fundamental rate		<table border="1"> <thead> <tr> <th>Value (bin)</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>48 kHz</td> </tr> <tr> <td>01</td> <td>44.1 kHz</td> </tr> <tr> <td>10</td> <td>32 kHz</td> </tr> <tr> <td>11</td> <td>Illegal or no input detected</td> </tr> </tbody> </table>	Value (bin)	Interpretation	00	48 kHz	01	44.1 kHz	10	32 kHz	11	Illegal or no input detected	2:0	Audio transmitter state (TBD)
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	<table border="1"> <thead> <tr> <th>Value (bin)</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>48 kHz</td> </tr> <tr> <td>01</td> <td>44.1 kHz</td> </tr> <tr> <td>10</td> <td>32 kHz</td> </tr> <tr> <td>11</td> <td>Illegal or no input detected</td> </tr> </tbody> </table>	Value (bin)	Interpretation	00	48 kHz	01	44.1 kHz	10	32 kHz	11	Illegal or no input detected																											
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2:0	Audio transmitter state (TBD)																																					

² For 2x rates (96,88.2,64kHz) every second sample is discarded in ATX, and in ARX the remaining samples are output at 1x rate.



0x02	INTSTA	R	0x00	<p>Read interrupt status. Clear interrupt source bits that are read out.</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Reserved, do not use</td> </tr> <tr> <td>6</td> <td>link broken status flag</td> </tr> <tr> <td>5</td> <td>poor link quality status flag</td> </tr> <tr> <td>4</td> <td>remote transfer done status flag</td> </tr> <tr> <td>3</td> <td>remote input changed status flag</td> </tr> <tr> <td>2:0</td> <td>Reserved, do not use</td> </tr> </tbody> </table> <p>See INTCF for interrupt enabling</p>	Bit	Interpretation	7	Reserved, do not use	6	link broken status flag	5	poor link quality status flag	4	remote transfer done status flag	3	remote input changed status flag	2:0	Reserved, do not use												
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0x1A	TXMOD	R/W	0x81	<p>Set operation modes for audio transmitter</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Transmitter enable</td> </tr> <tr> <td>6</td> <td>Audio transmitter power down</td> </tr> <tr> <td>5</td> <td>Enable wakeup on changing DD[1]</td> </tr> <tr> <td>4</td> <td>REQ pin polarity (0 for active low)</td> </tr> <tr> <td>3</td> <td>Enable direct data from pins DD[2:0]. DD[2] is only available if SSEL=1</td> </tr> <tr> <td>2</td> <td>S/PDIF enable (default input is I2S)</td> </tr> <tr> <td>1:0</td> <td>MCLK output control see also ch.3.4.</td> </tr> <tr> <td></td> <td>Value (bin) Interpretation</td> </tr> <tr> <td></td> <td>00 MCLK off (logic 0)</td> </tr> <tr> <td></td> <td>01 Output 256 x 48 kHz</td> </tr> <tr> <td></td> <td>10 Output 256 x 44.1 kHz</td> </tr> <tr> <td></td> <td>11 Output 256 x 32 kHz</td> </tr> </tbody> </table>	Bit	Interpretation	7	Transmitter enable	6	Audio transmitter power down	5	Enable wakeup on changing DD[1]	4	REQ pin polarity (0 for active low)	3	Enable direct data from pins DD[2:0]. DD[2] is only available if SSEL=1	2	S/PDIF enable (default input is I2S)	1:0	MCLK output control see also ch.3.4.		Value (bin) Interpretation		00 MCLK off (logic 0)		01 Output 256 x 48 kHz		10 Output 256 x 44.1 kHz		11 Output 256 x 32 kHz
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0x11	TXFMT	R/W	0x00	<p>Transmit data format (TBD)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>16 bit linear PCM</td> </tr> <tr> <td>1</td> <td>24 bit linear companded to 16 bit</td> </tr> <tr> <td>2</td> <td>16 bit linear companded to 12 bit</td> </tr> <tr> <td>4</td> <td>16 bit linear companded to 8 bit</td> </tr> </tbody> </table>	Value	Interpretation	0	16 bit linear PCM	1	24 bit linear companded to 16 bit	2	16 bit linear companded to 12 bit	4	16 bit linear companded to 8 bit																
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0x12	TXLAT	R/W	0x00	<p>ATX to ARX Latency</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Nominal, 10ms @ 48kHz</td> </tr> <tr> <td>1</td> <td>High, TBD ms @ 48kHz</td> </tr> <tr> <td>2</td> <td>Low, 5 ms @ 48kHz</td> </tr> </tbody> </table>	Value	Interpretation	0	Nominal, 10ms @ 48kHz	1	High, TBD ms @ 48kHz	2	Low, 5 ms @ 48kHz																		
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1	High, TBD ms @ 48kHz																													
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nRF24Z1 wireless audio streamer

0x20	TXDD	R	0x00	Value of ATX DD input pins	
				Bit	Interpretation
				7:3	Reserved, do not use
				2	Value of DD2 (only if SSEL=1)
				1	Value of DD1
0	Value of DD0				
0x13	INTCF	R/W	0x00	Interrupt configuration. Select events that can generate interrupt on the IRQ pin.	
				Bit	Interpretation
				7	Interrupt polarity, 1 is active high
				6	Enable link broken interrupt
				5	Enable poor link quality interrupt
				4	Enable remote transfer done interrupt
				3	Enable remote input changed interrupt
2:0	Reserved, MBZ				



0x14	I2SCNF_IN	R/W	0x00	I2S interface configuration for audio input (on ATX side), see also Table 10-1	
				Bit	Interpretation
				7	Data enable
					Value Interpretation
					0 I2S carries sound
					1 I2S carries data
				6	Reserved, MBZ
				5:4	Sample length
					Value Interpretation
					00 16-bit samples
	01 reserved				
	10 24-bit samples				
	11 reserved				
3	WS Polarity				
	Value Interpretation				
	0 WS=0: Left sample (std)				
	1 WS=1: Left sample				
2	Data to Bit Clock relation (data valid at clock edge)				
	Value Interpretation				
	0 Rising Edge (standard)				
	1 Falling Edge				
1	WS to MSB delay				
	Value Interpretation				
	0 1 clock cycle (standard)				
	1 0 clock cycles				
0	Audio word justification				
	Value Interpretation				
	0 Left justified				
	1 Right justified				
0x15	I2SRAT	R/W	0x00	I2S interface speed for digital input streams that are not interpreted as audio by nRF24Z1.	
				Value	Interpretation
				(n dec)	Digital stream
				0	8 kbit/s
				1	16 kbit/s
				2-254	(n+1)*8 kbit/s
255	2048 kbit/s				



0x16	TXPWR	R/W	0x03	Audio transmitter output power	
				Value	Interpretation
				0	-20 dBm
				1	-10 dBm
				2	-5 dBm
3	0 dBm				
0x17	TXSTI[0]	R/W	0x00	Audio transmitter (and link) sleep timer byte #0 TXSTI is a 16-bit number specifying the number of 10 ms (nominal) periods the audio transmitter should sleep between attempting to establish a new link.	
0x18	TXSTI[1]	R/W	0x00	Audio transmitter sleep timer byte #1	
0x19	TXWTI	R/W	0x00	Audio transmitter wake timer. With TXWTI set to 0, the audio transmitter will not go back to power down mode. A number larger than 0 will specify the number of 10ms (nominal) periods before the audio transmitter will reenter power down mode.	
0x10	TXRESO	R/W	0x00	Optional RESET pulse output from ATX may be enabled. Pulse length TBD.	
				Bit	Interpretation
				7:3	Reserved, MBZ
				2:1	0 : no RESET output 1 : RESET output on MSDA pin 2 : RESET output on MOSI pin 3 : RESET output on SPDIO pin
0	ATX RESET output polarity 0 : active low 1 : active high length of reset pulse is ca 285us				
0x1B	TXCSTATE	R/W	0x00	ATX config registers state (registers 0x10 to 0x1A) 0 : ATX config registers free to be used. 1 : ATX config registers may not be accessed Setting TXCSTATE=1 tells ATX to send ATX config registers values to ARX, and TXSTATE will be reset to 0 by ATX upon successful transfer to ARX. Then ATX will break link and relink. An external MCU should poll this register before accessing any ATX config register.	

3.2 Link configuration registers

The set of link configuration registers are located in the audio transmitter address map, but the QoS module on both sides of the link maintains synchronized copies.



Address Hex	Register	R/W	Initial Hex	Description												
0x03	LNKSTA	R	0x00	<p>Link status register</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7:6</td> <td>Reserved, do not use</td> </tr> <tr> <td>5</td> <td>LNKERR Changed</td> </tr> <tr> <td>4</td> <td>LNKQ Changed</td> </tr> <tr> <td>3:1</td> <td>Reserved, do not use</td> </tr> <tr> <td>0</td> <td>Link established</td> </tr> </tbody> </table>	Bit	Interpretation	7:6	Reserved, do not use	5	LNKERR Changed	4	LNKQ Changed	3:1	Reserved, do not use	0	Link established
Bit	Interpretation															
7:6	Reserved, do not use															
5	LNKERR Changed															
4	LNKQ Changed															
3:1	Reserved, do not use															
0	Link established															
0x04	LNKQ	R	0x00	<p>Link quality register. Number of successfully transmitted packets per unit of time. A value of 0 means all packets out of 256 are lost, a value of 128 means that 50% of the packets were lost and a value of 255 means that no packet out of 256 is lost. This number always represents the status over the last 256 packets transmitted. A packet consists of 16 samples, which is about 85 ms at a sampling rate of 48kHz.</p>												
0x05	LNKERR	R	0x00	<p>Link error register. Number of audio packets permanently lost per unit of time. A packet is permanently lost if it's not successfully received at the time its required at the audio output.</p>												



0x30	LNKMOD	R/W	0x00	Link mode register.	
				Bit	Interpretation
				7	ATX and ARX may also use broadcast values of B_CHP, B_ALEN and B_ADDR registers to establish link.
				6	ATX and ARX may load initial register values from EEPROM on relink.
				5	Link Standby mode
				4	Reserved, MBZ.
				3:2	Action when LNKERR > LNKETH
					Value Interpretation
					00 Break link
					01 Reserved, MBZ
	10 Reserved, MBZ				
	11 No action				
	1:0	Action when LNKQ > LNKWTH			
		Value Interpretation			
		00 Break link			
		01 Reserved, MBZ			
		10 Reserved, MBZ			
		11 No action			
0x31	LNKWTH	R/W	0xff	Link warning threshold limit. A LNKQ value \geq LNKWTH will cause IRQ to be activated (if enabled by INTCF.5)	
0x32	LNKETH	R/W	0xff	Link error threshold limit. A LNKERR value \geq LNKETH will cause IRQ to be activated (if enabled by INTCF.6)	
0x25	B_CHP1	R/W	0x01	The following registers with prefix B_ (as compared to similar registers described below) refer to broadcast values for frequency hopping and device address. These values may be common to a group of devices. B_CHP1 is minimum channel number for frequency hopping ³ , see also ch. 3.5	
0x26	B_CHP2	R/W	0x12	Maximum channel number for frequency hopping, see also ch. 3.5	
0x27	B_CHP3	R/W	0x05	Step channel number for frequency hopping, see also ch. 3.5	

³ All channels are entered as a 7-bit number which represents the number of 4-MHz increments above 2400MHz. If CHP3=0 frequency hopping is disabled. New values in CHP1,CHP2,CHP3 registers will be used next time a new link is established., which implies that frequency hopping scheme may not be changed, without breaking current link.



0x28	B_ALEN	R/W	0x05	Address length in bytes, legal range is 4 or 5
0x29	B_ADDR[0]	R/W	0x01	Address byte #0 (LSB)
0x2A	B_ADDR[1]	R/W	0x02	Address byte #1
0x2B	B_ADDR[2]	R/W	0x03	Address byte #2
0x2C	B_ADDR[3]	R/W	0x04	Address byte #3
0x2D	B_ADDR[4]	R/W	0x05	Address byte #4 (don't care if ALEN =4)
0x35	CHP1	R/W	0x01	The following registers without any prefix (as compared to the B_registers mentioned above) are the individual setting for each pair of devices for frequency hopping and device address. CHP1 is minimum channel number for frequency hopping ³ , see also ch. 3.5
0x36	CHP2	R/W	0x12	Maximum channel number for frequency hopping, see also ch. 3.5
0x37	CHP3	R/W	0x05	Step channel number for frequency hopping, see also ch. 3.5
0x38	ALEN	R/W	0x05	Address length in bytes, legal range is 4 or 5
0x39	ADDR[0]	R/W	0x01	Address byte #0 (LSB)
0x3A	ADDR[1]	R/W	0x02	Address byte #1
0x3B	ADDR[2]	R/W	0x03	Address byte #2
0x3C	ADDR[3]	R/W	0x04	Address byte #3
0x3D	ADDR[4]	R/W	0x05	Address byte #4 (don't care if ALEN =4)
0x3E	LNKCSTATE	R/W	0x00	Link config registers state (registers 0x30 to 0x3D) 0 : Link config registers free to be used. 1 : Link config registers may not be accessed Setting LNKCSTATE=1 tells ATX to send Link config registers values to ARX, and LNKCSTATE will be reset to 0 by ATX upon successful transfer to ARX. Then ATX will break link and relink. An external MCU should poll this register before accessing any Link config register.

3.3 Audio receiver access registers

These registers are used to access the IO pins on the audio receiver and the two master serial interfaces on the audio receiver for example for volume control, switch or indicator control. It's also possible to inquire the state of the audio receiver parallel inputs or read data from audio receiver SPI or 2-wire masters. Note that the access to these registers are done via the serial interface of the audio transmitter.



Address Hex	Register	R/W	Initial Hex	Description																		
0x06	RXSTA	R	0x00	Reserved, do not use																		
0x4A	RXMOD	R/W	0x80	Set operation modes for audio receiver <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Receiver power down</td> </tr> <tr> <td>6</td> <td>MCLK direction control, should be set to 0 (output)</td> </tr> <tr> <td>5</td> <td>Reserved, MBZ</td> </tr> <tr> <td>4</td> <td>REQ pin polarity</td> </tr> <tr> <td>3</td> <td>Reserved, MBZ</td> </tr> <tr> <td>2</td> <td>S/PDIF enable</td> </tr> <tr> <td>1:0</td> <td>Reserved, MBZ</td> </tr> </tbody> </table>	Bit	Interpretation	7	Receiver power down	6	MCLK direction control, should be set to 0 (output)	5	Reserved, MBZ	4	REQ pin polarity	3	Reserved, MBZ	2	S/PDIF enable	1:0	Reserved, MBZ		
Bit	Interpretation																					
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4	REQ pin polarity																					
3	Reserved, MBZ																					
2	S/PDIF enable																					
1:0	Reserved, MBZ																					
0x41	RXPIO	R/W	0x00	Receiver GPIO output and drive strength <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>High drive enable for DO[3]</td> </tr> <tr> <td>6</td> <td>High drive enable for DO[2]</td> </tr> <tr> <td>5</td> <td>High drive enable for DO[1]</td> </tr> <tr> <td>4</td> <td>High drive enable for DO[0]</td> </tr> <tr> <td>3</td> <td>Data for DO[3]</td> </tr> <tr> <td>2</td> <td>Data for DO[2]</td> </tr> <tr> <td>1</td> <td>Data for DO[1]</td> </tr> <tr> <td>0</td> <td>Data for DO[0]</td> </tr> </tbody> </table>	Bit	Interpretation	7	High drive enable for DO[3]	6	High drive enable for DO[2]	5	High drive enable for DO[1]	4	High drive enable for DO[0]	3	Data for DO[3]	2	Data for DO[2]	1	Data for DO[1]	0	Data for DO[0]
Bit	Interpretation																					
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5	High drive enable for DO[1]																					
4	High drive enable for DO[0]																					
3	Data for DO[3]																					
2	Data for DO[2]																					
1	Data for DO[1]																					
0	Data for DO[0]																					
0x42	RXPWME	R/W	0x00	Enables audio receiver PWM onto DO[3] and set PWM frequency <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7:6</td> <td>00 : PWM not enabled 11 : Enable PWM on DO[3] 01,10 : reserved, do not use</td> </tr> <tr> <td>5:0</td> <td>PWM frequency (repetition rate) $f_{\text{PWM}} = 16\text{MHz} / (255 * (1 + \text{RXPWME}[5:0]))$</td> </tr> </tbody> </table>	Bit	Interpretation	7:6	00 : PWM not enabled 11 : Enable PWM on DO[3] 01,10 : reserved, do not use	5:0	PWM frequency (repetition rate) $f_{\text{PWM}} = 16\text{MHz} / (255 * (1 + \text{RXPWME}[5:0]))$												
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5:0	PWM frequency (repetition rate) $f_{\text{PWM}} = 16\text{MHz} / (255 * (1 + \text{RXPWME}[5:0]))$																					
0x43	RXPWMD	R/W	0x00	Set audio receiver PWM duty cycle																		



Address Hex	Register	R/W	Initial Hex	Description																																																		
0x44	I2SCNF_OUT	R/W	0x00	<p>I2S interface configuration for audio output (on ARX side), see also Table 10-1</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Reserved, MBZ</td> </tr> <tr> <td>6</td> <td>Mute sound output</td> </tr> <tr> <td>5:4</td> <td>Sample length</td> </tr> <tr> <td></td> <td>Value Interpretation</td> </tr> <tr> <td></td> <td>00 16-bit samples</td> </tr> <tr> <td></td> <td>01 reserved</td> </tr> <tr> <td></td> <td>10 24-bit samples</td> </tr> <tr> <td></td> <td>11 reserved</td> </tr> <tr> <td>3</td> <td>WS Polarity</td> </tr> <tr> <td></td> <td>Value Interpretation</td> </tr> <tr> <td></td> <td>0 WS=0: Left sample (std)</td> </tr> <tr> <td></td> <td>1 WS=1: Left sample</td> </tr> <tr> <td>2</td> <td>Data to Bit Clock relation (data valid at clock edge)</td> </tr> <tr> <td></td> <td>Value Interpretation</td> </tr> <tr> <td></td> <td>0 Rising Edge (standard)</td> </tr> <tr> <td></td> <td>1 Falling Edge</td> </tr> <tr> <td>1</td> <td>WS to MSB delay</td> </tr> <tr> <td></td> <td>Value Interpretation</td> </tr> <tr> <td></td> <td>0 1 clock cycle (standard)</td> </tr> <tr> <td></td> <td>1 0 clock cycles</td> </tr> <tr> <td>0</td> <td>Audio word justification</td> </tr> <tr> <td></td> <td>Value Interpretation</td> </tr> <tr> <td></td> <td>0 Left justified</td> </tr> <tr> <td></td> <td>1 Right justified</td> </tr> </tbody> </table>	Bit	Interpretation	7	Reserved, MBZ	6	Mute sound output	5:4	Sample length		Value Interpretation		00 16-bit samples		01 reserved		10 24-bit samples		11 reserved	3	WS Polarity		Value Interpretation		0 WS=0: Left sample (std)		1 WS=1: Left sample	2	Data to Bit Clock relation (data valid at clock edge)		Value Interpretation		0 Rising Edge (standard)		1 Falling Edge	1	WS to MSB delay		Value Interpretation		0 1 clock cycle (standard)		1 0 clock cycles	0	Audio word justification		Value Interpretation		0 Left justified		1 Right justified
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0x07	RXPIN	R	0x00	<p>Current state of audio receiver GPIO inputs</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7:4</td> <td>Reserved, do not use.</td> </tr> <tr> <td>3</td> <td>DI3 value</td> </tr> <tr> <td>2</td> <td>DI2 value</td> </tr> <tr> <td>1</td> <td>DI1 value</td> </tr> <tr> <td>0</td> <td>DI0 value</td> </tr> </tbody> </table>	Bit	Interpretation	7:4	Reserved, do not use.	3	DI3 value	2	DI2 value	1	DI1 value	0	DI0 value																																						
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Address Hex	Register	R/W	Initial Hex	Description																
0x45	RXWAKE	R/W	0x28	<p>Wakeup sources for audio receiver</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7:6</td> <td>Reserved, MBZ</td> </tr> <tr> <td>5</td> <td>Goto powerdown mode on DI3 change</td> </tr> <tr> <td>4</td> <td>Wakeup on sleep timer</td> </tr> <tr> <td>3</td> <td>Wakeup on DI3 change</td> </tr> <tr> <td>2</td> <td>Wakeup on DI2 change</td> </tr> <tr> <td>1</td> <td>Wakeup on DI1 change</td> </tr> <tr> <td>0</td> <td>Wakeup on DI0 change</td> </tr> </tbody> </table>	Bit	Interpretation	7:6	Reserved, MBZ	5	Goto powerdown mode on DI3 change	4	Wakeup on sleep timer	3	Wakeup on DI3 change	2	Wakeup on DI2 change	1	Wakeup on DI1 change	0	Wakeup on DI0 change
Bit	Interpretation																			
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2	Wakeup on DI2 change																			
1	Wakeup on DI1 change																			
0	Wakeup on DI0 change																			
0x49	RXPWR	R/W	0x00	<p>Audio receiver output power</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>-20 dBm</td> </tr> <tr> <td>1</td> <td>-10 dBm</td> </tr> <tr> <td>2</td> <td>-5 dBm</td> </tr> <tr> <td>3</td> <td>0 dBm</td> </tr> </tbody> </table>	Value	Interpretation	0	-20 dBm	1	-10 dBm	2	-5 dBm	3	0 dBm						
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2	-5 dBm																			
3	0 dBm																			
0x46	RXSTI[0]	R/W	0x00	<p>Audio receiver sleep timer byte #0 RXSTI is a 16-bit number specifying the number of 10 ms (nominal) periods the audio receiver should sleep between attempting to establish a new link. Only used if sleep timer is enabled, see bit 4 of RWAKE register.</p>																
0x47	RXSTI[1]	R/W	0x00	<p>Audio receiver sleep timer byte #1</p>																
0x48	RXWTI	R/W	0x00	<p>Audio receiver wake timer. With RXWTI set to 0, the audio receiver will not go back to power down mode. A number larger than 0 will specify the number of 10ms (nominal) periods before the audio receiver will reenter power down mode.</p>																
0x40	RXRESO	R/W	0x00	<p>Optional RESET pulse output from ARX may be enabled. Pulse length TBD.</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7:3</td> <td>Reserved, MBZ</td> </tr> <tr> <td>2:1</td> <td> 0 : no RESET output 1 : RESET output on MSDA pin 2 : RESET output on MOSI pin 3 : RESET output on SPDIO pin </td> </tr> <tr> <td>0</td> <td> ARX RESET output polarity 0 : active low 1 : active high length of reset pulse is ca 285us </td> </tr> </tbody> </table>	Bit	Interpretation	7:3	Reserved, MBZ	2:1	0 : no RESET output 1 : RESET output on MSDA pin 2 : RESET output on MOSI pin 3 : RESET output on SPDIO pin	0	ARX RESET output polarity 0 : active low 1 : active high length of reset pulse is ca 285us								
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Address Hex	Register	R/W	Initial Hex	Description
0x4B	RXCSTATE	R/W	0x00	ARX config registers state (registers 0x40 to 0x4A) 0 : ARX config registers free to be used. 1 : ARX config registers may not be accessed Setting RXCSTATE=1 tells ATX to send all ARX config registers values to ARX, and RXSTATE will be reset to 0 by ATX upon successful transfer to ARX. An external MCU should poll this register before accessing any ARX config register.



Address Hex	Register	R/W	Initial Hex	Description																																																																						
0x70	RXDCMD	R/W	0x82	<p>Data “command”. Specifies interface and speed</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Interface select <table border="1"> <thead> <tr> <th>Value</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use 2-wire interface</td> </tr> <tr> <td>1</td> <td>Use SPI interface</td> </tr> </tbody> </table> </td> </tr> <tr> <td>6:4</td> <td>SPI slave select control. Set which signal to be used as slave select, and associated polarity. Or 2-wire access type. <table border="1"> <thead> <tr> <th>Value</th> <th>SPI interpretation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>CSN, active low²</td> </tr> <tr> <td>001</td> <td>DO[0], active low¹</td> </tr> <tr> <td>010</td> <td>DO[1], active low¹</td> </tr> <tr> <td>011</td> <td>DO[2], active low¹</td> </tr> <tr> <td>100</td> <td>CSN, active low²</td> </tr> <tr> <td>101</td> <td>DO[0], active high¹</td> </tr> <tr> <td>110</td> <td>DO[1], active high¹</td> </tr> <tr> <td>111</td> <td>DO[2], active high¹</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>2-wire interpretation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>start stop access</td> </tr> <tr> <td>001</td> <td>start only access (a start only access followed by a start-stop access will be a start-start-stop access)</td> </tr> </tbody> </table> </td> </tr> <tr> <td>3:1</td> <td>Speed select <table border="1"> <thead> <tr> <th>Value (bin)</th> <th>SPI Interpretation</th> <th>2-wire Interpretation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8 Mbit/s</td> <td>Illegal</td> </tr> <tr> <td>001</td> <td>8 Mbit/s</td> <td>100 kbit/s</td> </tr> <tr> <td>010</td> <td>4 Mbit/s</td> <td>400 kbit/s</td> </tr> <tr> <td>011</td> <td>2 Mbit/s</td> <td>1 Mbit/s</td> </tr> <tr> <td>100</td> <td>1 Mbit/s</td> <td>Illegal</td> </tr> <tr> <td>101</td> <td>500 kbit/s</td> <td>Illegal</td> </tr> <tr> <td>110</td> <td>250 kbit/s</td> <td>Illegal</td> </tr> <tr> <td>111</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> </td> </tr> <tr> <td>0</td> <td>Reserved, MBZ.</td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>Notes:</p> <ol style="list-style-type: none"> In order to use any of DO[2:0] as slave selects, the corresponding bit in RXPIO should be set to the inactive state of the corresponding slave select MCSN is always active low 	Bit	Interpretation	7	Interface select <table border="1"> <thead> <tr> <th>Value</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use 2-wire interface</td> </tr> <tr> <td>1</td> <td>Use SPI interface</td> </tr> </tbody> </table>	Value	Interpretation	0	Use 2-wire interface	1	Use SPI interface	6:4	SPI slave select control. Set which signal to be used as slave select, and associated polarity. Or 2-wire access type. <table border="1"> <thead> <tr> <th>Value</th> <th>SPI interpretation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>CSN, active low²</td> </tr> <tr> <td>001</td> <td>DO[0], active low¹</td> </tr> <tr> <td>010</td> <td>DO[1], active low¹</td> </tr> <tr> <td>011</td> <td>DO[2], active low¹</td> </tr> <tr> <td>100</td> <td>CSN, active low²</td> </tr> <tr> <td>101</td> <td>DO[0], active high¹</td> </tr> <tr> <td>110</td> <td>DO[1], active high¹</td> </tr> <tr> <td>111</td> <td>DO[2], active high¹</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>2-wire interpretation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>start stop access</td> </tr> <tr> <td>001</td> <td>start only access (a start only access followed by a start-stop access will be a start-start-stop access)</td> </tr> </tbody> </table>	Value	SPI interpretation	000	CSN, active low ²	001	DO[0], active low ¹	010	DO[1], active low ¹	011	DO[2], active low ¹	100	CSN, active low ²	101	DO[0], active high ¹	110	DO[1], active high ¹	111	DO[2], active high ¹	Value	2-wire interpretation	000	start stop access	001	start only access (a start only access followed by a start-stop access will be a start-start-stop access)	3:1	Speed select <table border="1"> <thead> <tr> <th>Value (bin)</th> <th>SPI Interpretation</th> <th>2-wire Interpretation</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8 Mbit/s</td> <td>Illegal</td> </tr> <tr> <td>001</td> <td>8 Mbit/s</td> <td>100 kbit/s</td> </tr> <tr> <td>010</td> <td>4 Mbit/s</td> <td>400 kbit/s</td> </tr> <tr> <td>011</td> <td>2 Mbit/s</td> <td>1 Mbit/s</td> </tr> <tr> <td>100</td> <td>1 Mbit/s</td> <td>Illegal</td> </tr> <tr> <td>101</td> <td>500 kbit/s</td> <td>Illegal</td> </tr> <tr> <td>110</td> <td>250 kbit/s</td> <td>Illegal</td> </tr> <tr> <td>111</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value (bin)	SPI Interpretation	2-wire Interpretation	000	8 Mbit/s	Illegal	001	8 Mbit/s	100 kbit/s	010	4 Mbit/s	400 kbit/s	011	2 Mbit/s	1 Mbit/s	100	1 Mbit/s	Illegal	101	500 kbit/s	Illegal	110	250 kbit/s	Illegal	111	Reserved	Reserved	0	Reserved, MBZ.			
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Address Hex	Register	R/W	Initial Hex	Description
0x71	RXWCNT	R/W	0x00	Number of bytes to write (max 16)
0x72	RXRCNT	R/W	0x00	Number of bytes to read (max 16)
0x50-0x5f	RXWBUF	W	0x00	Data to be written to the interface specified by RXCMD
0x60-0x6f	RXRBUF	R	0x00	Data read from audio receiver on the interface specified by RXCMD
0x74	RXEXEC	W/R	0x00	Write to this register will execute a command on the audio receiver. The interface and speed are specified by RXCMD. The audio receiver will first write RXWCNT bytes from RXWBUF to the selected interface, then read RXRCNT bytes and transmit back to be stored in RXRBUF. An interrupt may be delivered upon successful completion of the command. 0= idle; 1=write or read MCU must set RXEXEC=1 to perform command, and can thereafter read RXEXEC to find if command is finished (idle)

3.4 ATX MCLK control

On ATX side MCLK may be output to be used to clock external devices like an ADC. For I2S audio input it is otherwise not needed.

For S/PDIF audio input, MCLK output is disabled, but even so the MCLK control value in register TXMOD should be set to the expected sampling frequency of the audio. This gives better phase margin and best result when an audio signal with much jitter is input. And for 32kHz this is the only alternative, i.e. 32kHz S/PDIF input requires that MCLK control is set to binary 11. However when MCLK control is set to binary 01 (48kHz), nRF24Z1 will be able to automatically detect if audio rate is 44.1 or 48kHz, so that it is not necessary to change MCLK control value when switching between 44.1 and 48 kHz S/PDIF input.

3.5 Frequency hopping

The channel jumping algorithm is based on three parameters. Start channel, end channel and channel step, which are set in registers CHP1, CHP2 and CHP3.

The formula is like this:

Start Channel – CHP1
End Channel – CHP2
Channel Step – CHP3
Present Channel – PCh

$PCh = PCh + CHP3$
if ($PCh > CHP2$)



nRF24Z1 wireless audio streamer

$$PCh = PCh - (CHP2 - CHP1 + 4)$$

With these three parameters the user has the opportunity to make a custom frequency hopping. If the user shall use two systems in the same area it's important that the user chooses two different frequency hopping systems. In nRF24Z1 you have the opportunity to choose channels with 4 MHz spacing.

nRF24Z1 has no adaptive frequency hopping. It hops every time the audio transmitter sends a burst. The user has to consider frequency hopping up against Wireless LAN. A WLAN will use 20 MHz to transmit. Because of this fact it can be advantageous to set the frequency hopping step a little larger than 4 channels. This will avoid the WLAN two out of three times.



4 INTERFACE TIMING

4.1 I2S input (audio transmitter) timing

The I2S input protocol is configurable to handle different I2S sources. In addition, the interface will automatically detect sample size and word length for the most common formats. This section shows the detailed bit, clock and word timing requirements.

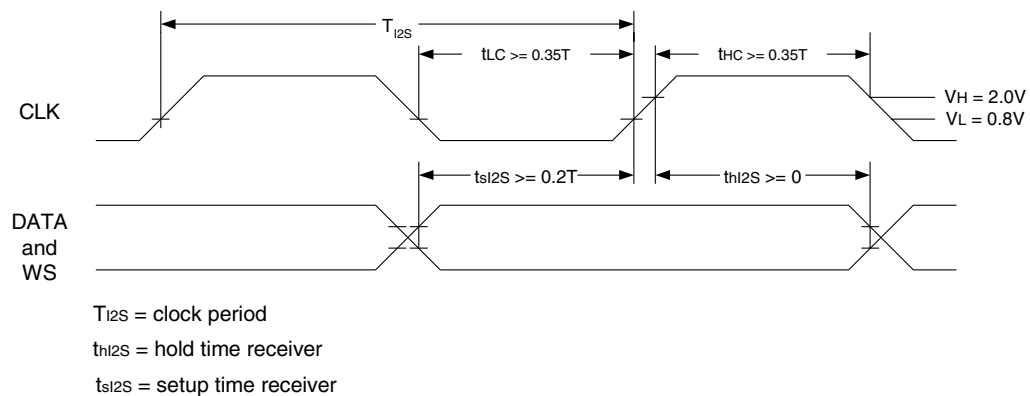


Figure 4-1. Timing for I2S input on nRF24Z1 audio transmitter

4.2 I2S output (audio receiver) timing

I2S output is protocol compatible with most I2S DACs and CODECs. This section shows the detailed bit, clock and word timing requirements.

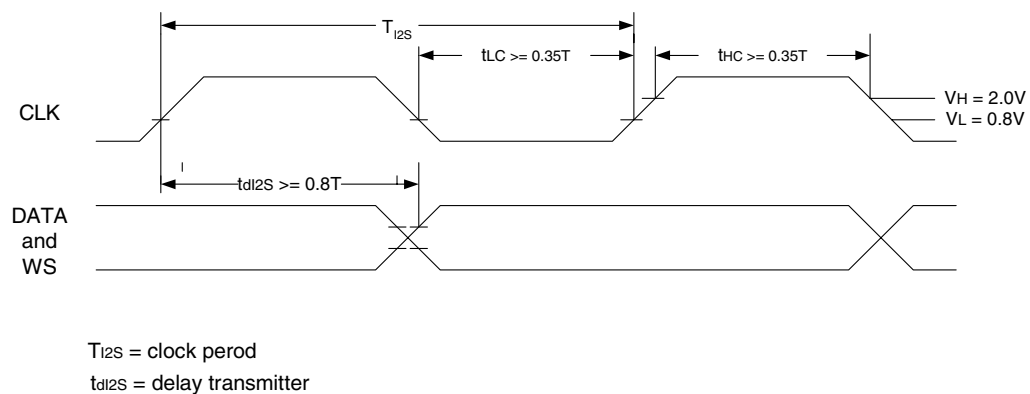


Figure 4-2. Timing for I2S output on nRF24Z1 audio receiver

4.3 SPI master timing

The slave(s) that are connected determines the protocol on the SPI master interface. For the case of memories, nRF24Z1 is protocol compatible with “industry standard” SPI memory with sizes ranging from 1 Kbyte to 64 Kbytes (16-bit sub-address used).

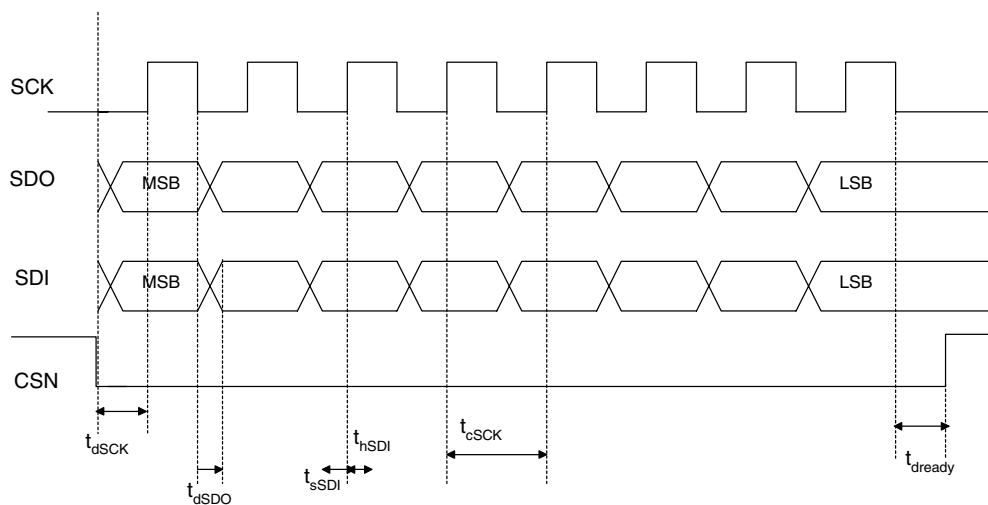


Figure 4-3 : SPI master interface timing, here is shown a one byte transaction.

t_{cSCK} : MSCK cycle time, as defined by RXDCMD register.

t_{dSCK} : time from M_{CSN} active to first SCK pulse,

$$t_{dSCK} = t_{cSCK} / 2$$

t_{dSDO} : delay from negege MSCK to new MMOSI output data, may vary from -40ns to 40ns

t_{sSDI} : MMISO setup time to posedge MSCK, $t_{sSDI} > 45\text{ns}$.

t_{hSDI} : MMISO hold time to posedge MSCK, $t_{hSDI} > 0\text{ns}$.

t_{dready} : time from last MSCK pulse to M_{CSN} goes inactive

$$t_{dready} = 7 \text{ CPU clock cycles}$$

4.4 SPI slave timing

The first byte of the SPI transaction is a “command” with an embedded sub-address specifying one of the registers described in section 3. The “command” also specifies if the remainder of the operation is read or write. Consecutive accesses with SCSN low will auto-increment the address. This means that all registers may theoretically be accessed with one SPI transfer.

4.5 2-wire master timing

The slave(s) that are connected determines the protocol on the 2-wire master interface. For the case of memories, nRF24Z1 is protocol compatible with “industry standard” 2-wire memory with sizes ranging from 128 bytes to 4 Kbytes (3 bit of “address” and one byte sub-address used).

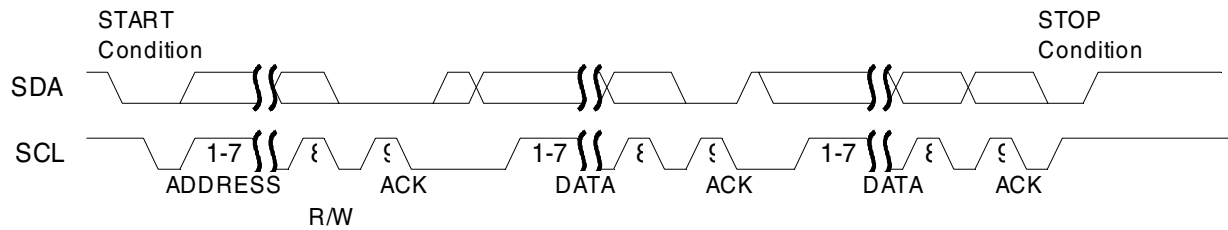


Figure 4-4 : 2-wire data transfer

4.6 2-wire slave timing

The first byte of the 2-wire transfer contains the address of nRF24Z1 and the read/write bit to give the direction of data transfer after the sub-address. The next byte of the 2-wires transaction is a “sub-address” specifying one of the registers described in section 3. Consecutive accesses without a stop condition will auto-increment the sub-address. This means that all registers may theoretically be accessed with one 2-wire transfer.

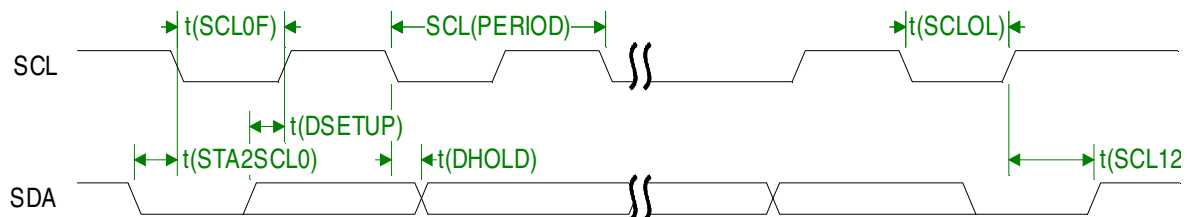


Figure 4-5 : 2-wire timing diagram, applies both to master and slave interface.



5 ANALOG INTERFACE

5.1 Antenna I/O

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either via a RF choke or via the center point in a balanced antenna. Differential load impedance between the ANT1 and ANT2 pins, $100\Omega + j175\Omega$, is recommended for maximum output power. Antennas with lower load impedance (for example 50Ω) can be matched to nRF24Z1 by using a simple matching network.

5.2 Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption TBC
11	0 dBm ± 3 dB	17 mA
10	-5 dBm ± 3 dB	15 mA
01	-10 dBm ± 3 dB	14 mA
00	-20 dBm ± 3 dB	13 mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27°C, Load impedance = $100\Omega + j175\Omega$.

Table 5-1 RF output power setting for nRF24Z1.

5.3 Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C _L	ESR	C _{0max}	Tolerance
16MHz	8pF – 16pF	100Ω	7.0pF	± 30 ppm

Table 5-2 Crystal specification of nRF24Z1

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying a lower value of crystal parallel equivalent capacitance, Co=1.5pF is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_max=7.0pF.

The crystal load capacitance, C_L, is given by:

$$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}, \quad \text{where } C_1' = C_1 + C_{PCB1} + C_{I1} \text{ and } C_2' = C_2 + C_{PCB2} + C_{I2}$$

C₁ and C₂ are 0603 SMD capacitors as shown in the application schematics. C_{PCB1} and C_{PCB2} are the layout parasitic on the circuit board. C_{I1} and C_{I2} are the capacitance seen into the XC1 and XC2 pin respectively; the value is typical 1pF.



6 ELECTRICAL SPECIFICATION

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Operating conditions						
AVDD	Supply voltage		2.0	3.0	3.6	V
TEMP	Operating temperature		-20	27	80	°C
Digital input pins						
V _{IH}	HIGH level input voltage		0.7 *AVDD		AVDD	V
V _{IL}	LOW level input voltage		AVSS		0.3*AVDD	V
Digital output pins						
V _{OH}	HIGH level output voltage (I _{OH} =-0.5mA)		AVDD-0.3		AVDD	V
V _{OL}	LOW level output voltage (I _{OL} =0.5mA)		AVSS		0.3	V
I _{OL_HD}	High drive sink current for DO[0] and DO[2] @ V _{OL} = 0.4V	1)			10	mA
I _{OH_HD}	High drive source current for DO[1] and DO[3] @ V _{OH} = VDD-0.4V	1)			10	mA
General electrical specification						
I _{PD}	Supply current in power down mode			4		µA
General RF conditions						
f _{OP}	Operating frequency	2)	2400		2521	MHz
f _{XTAL}	Crystal frequency			16		MHz
Δf	Frequency deviation			+/-640		kHz
R _{GFSK}	GFSK data rate			4000		kbps
f _{CHANNEL}	Channel spacing			4		MHz
RF Transmit mode						
P _{RF_0dBm}	Maximum output power (TXPWR=3)	3)		0	3	dBm
P _{RF_-5dBm}	Maximum output power (TXPWR=2)	3)		-5	0	dBm
P _{RF_-10dBm}	Maximum output power (TXPWR=1)	3)		-10	-5	dBm
P _{RF_-20dBm}	Maximum output power (TXPWR=0)	3)		-20	-12	dBm
P _{RFC}	RF power control range		16	20		dB
P _{RFCR}	RF power range control resolution				+/-3	dB
P _{BW}	20dB bandwidth for modulated carrier			4000		kHz
I _{TX_0dBm}	Supply current @ 0dBm output power			17		mA
I _{TX_-5dBm}	Supply current @ -5dBm output power			15		mA
I _{TX_-10dBm}	Supply current @ -10dBm output power			14		mA
I _{TX_-20dBm}	Supply current @ -20dBm output power			13		mA
RF Receive mode						
I _{RX}	Supply current in receive mode			32		mA
RX _{SENS}	Sensitivity at 0.1%BER			-80		dBm
RX _{MAX}	Maximum received signal		0			dBm
I2S interface timing						
T _{I2S}	I2S clock period		150			ns
t _{sI2S}	DATA and WS (input) setup time to CLK		20			ns
t _{hI2S}	DATA and WS (input) hold time from CLK		20			ns
t _{dI2S}	DATA and WS (output) delay from CLK				40	ns
S/PDIF interface timing						
	TBD					
MCLK (256 F_s) output clock						
Δf _{MCLK}	Deviation from nominal MCLK frequency	4)	-500		+500	ppm
J _{RMS}	RMS jitter 0-25kHz			250	310	ps



nRF24Z1 wireless audio streamer

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Slave SPI interface timing						
T_{SSCK}	SSCK clock period	5)	62			ns
t_{suSSPI}	SMOSI and SSCN setup time to SSCK		10			ns
t_{hdSSPI}	SMOSI and SSCN hold time from SSCK		10			ns
t_{dSSPI}	SMISO delay from SSCK (VDD > 2.5V)				25	ns
t_{dSSPI}	SMISO delay from SSCK (VDD > 2.0V)				50	ns
t_{suSCSN}	SCSN setup time to SSCK		10			ns
Master SPI interface timing						
t_{eSCK}	MSCK clock period		125			ns
t_{sSDI}	MMISO setup time to MSCK		10			ns
t_{hSDI}	MMISO hold time from MSCK		10			ns
t_{dSDO}	MMOSI delay from MSCK (VDD > 2.5V)				20	ns
t_{dSCK}	MCSN setup to MSCK		30	500		ns
2-wire interface timing						
$T_{SCL(PERIOD)}$	2-wire clock period		1000			ns
$t_{(D)SETUP}$	SSDA/MSDA setup time to SSCL/MSCL		55			ns
$t_{(D)HOLD}$	SSDA/MSDA hold time from SSCL/MSCL		50			ns
t_{pdhlW2}	SSDA/MSDA 1->0 delay from SSCL/MSCL				50	ns

Table 6-1 nRF24Z1 electrical specification.

- 1) Output pin programmed for high current (register RXPIO)
- 2) Operates in the 2400 MHz ISM band, 2400-2483 MHz,
- 3) Antenna load impedance = $100\Omega + j175\Omega$, please see peripheral RF information
- 4) Nominal MCLK frequency is 256 times f_s for f_s in [32kHz, 44.1kHz, 48kHz] programmable
- 5) For VDD 3.0V +/-10%, otherwise minimum T_{SSCK} is 124ns (8MHz)



7 PIN ASSIGNMENT

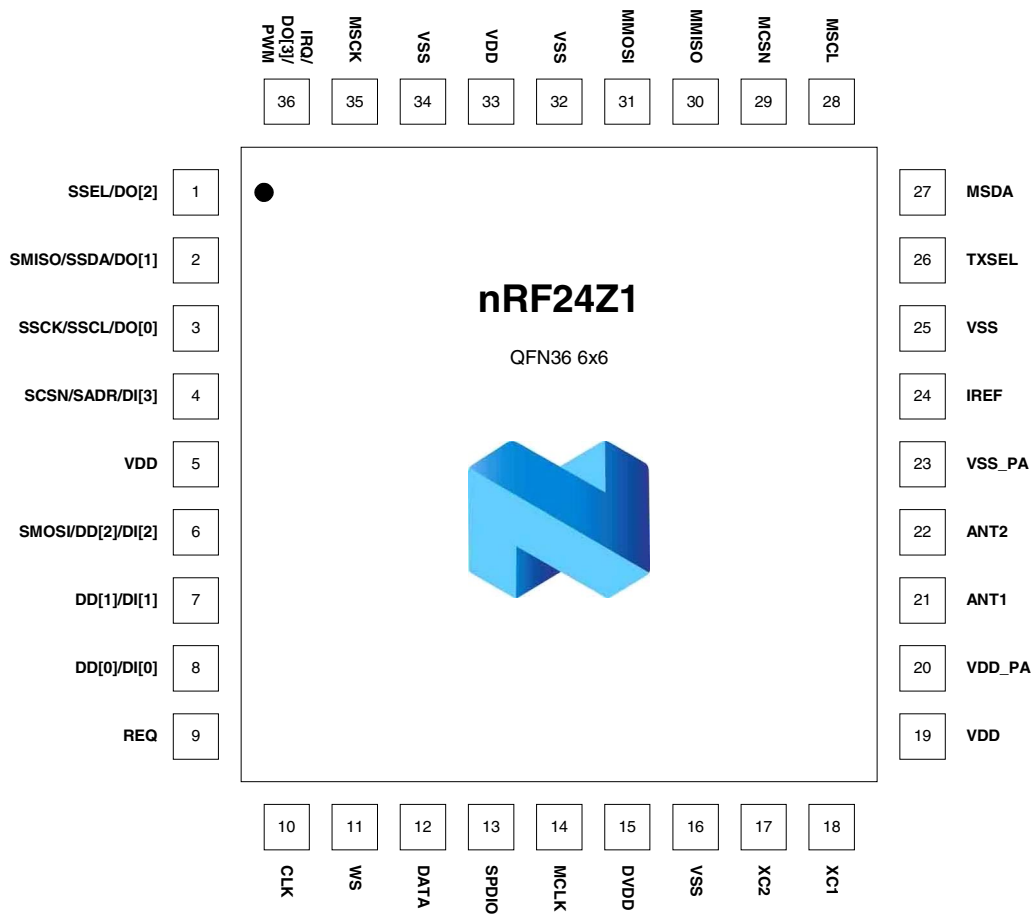


Figure 7-1: Pin assignment nRF24Z1



8 PIN FUNCTION

Pin	Name		Pin function		Description	
	Transm	Rec.	Transmit	Rec.	Transmit	Receive
1	SSEL	DO[2]	Dig. In	Dig. Out	Slave interface select 1: 2-wire, 0: SPI	GPIO out bit #2
2	SMISO /SSDA	DO[1]	Digital Output / Digital IO		Slave SPI serial out / Slave 2-wire data (bidir)	GPIO out bit #1
3	SSCK /SSCL	DO[0]	Dig. In	Dig. Out	Slave SPI clock / Slave 2-wire clock	GPIO out bit #0
4	SCSN /SADR	DI3	Digital Input		Slave SPI slave select / Address select 2-wire slave	GPIO in bit #2
5	VDD		Power		Power Supply (2.0-3.6 V DC)	
6	SMOSI /DD[2]	DI2	Digital Input		Slave SPI serial in / Direct data in bit #2	GPIO in bit #3
7	DD[1]	DI1	Digital Input		Direct data in bit #1	GPIO in bit #1
8	DD[0]	DI0	Digital Input		Direct data in bit #0	GPIO in bit #0
9	REQ		Dig. Out	Dig. In	I2S data request (programmable polarity)	
10	CLK		Dig. In	Dig. Out	I2S bit clock	
11	WS		Dig. In	Dig. Out	I2S word clock	
12	DATA		Dig. In	Dig. Out	I2S data signal	
13	SPDIO		Dig. In	Dig. Out	S/PDIF interface	
14	MCLK		Dig. Out	Dig IO	256X sample rate clock to ADC / from or to DAC	
15	DVDD		Regulator output		Digital voltage regulator output for decoupling	
16	VSS		Power		Ground (0V)	
17	XC2		Analog output		Crystal Pin 2	
18	XC1		Analog input		Crystal Pin 1	
19	VDD		Power		Power Supply (2.0-3.6 V DC)	
20	VDD_PA		Regulator output		DC supply (+1.8V) for RF output (ANT1, ANT2) only	
21	ANT1		RF		Antenna interface 1	
22	ANT2		RF		Antenna interface 2	
23	VSS_PA		Power		Ground (0V)	
24	IREF		Analog input		Connection to external Bias reference resistor	
25	VSS		Power		Ground (0V)	
26	TXSEL		Digital Input		nRF24Z1 function 1 : audio transmitter, 0: audio receiver	
27	MSDA		Digital IO		Master 2-wire bi-directional data	
28	MSCL		Digital IO		Master 2-wire bi-directional clock	
29	MCSN		Digital Output		Master SPI primary slave select (active low)	
30	MMISO		Digital Input		Master SPI serial input	
31	MMOSI		Digital Output		Master SPI serial output	
32	VSS		Power		Ground (0V)	
33	VDD		Power		Power Supply (2.0-3.6 V DC)	
34	VSS		Power		Ground (0V)	
35	MSCK		Digital Output		Master SPI clock	
36	IRQ	DO[3] / PWM	Digital Output		Interrupt request	GPIO out bit #3 / PWM output

Table 8-1 nRF24Z1 pin function



9 PACKAGE OUTLINE

nRF24Z1 is packaged in a 36 pin 6 by 6 TQFN (all dimensions in mm).

Package Type		A	A ₁	A ₂	b	D/E	D ₁ /E ₁	e	J	K	L	R
Green QFN36 (6x6 mm)	Min	0.8	0.0	0.65	0.18	6 BSC	5.75 BSC	0.5 BSC	4.47	4.47	0.3	1.735
	typ.		0.02		0.23				4.57	4.57	0.4	1.835
	Max	0.9	0.05	0.69	0.3				4.67	4.67	0.5	1.935

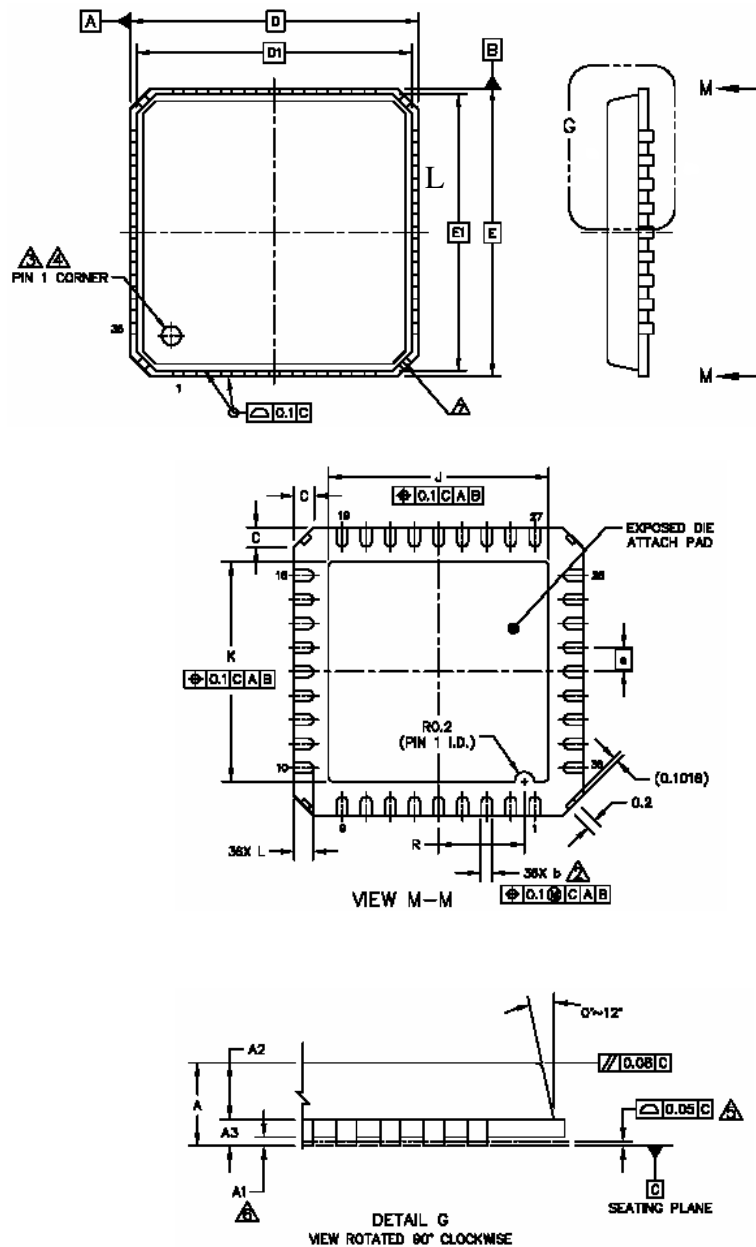
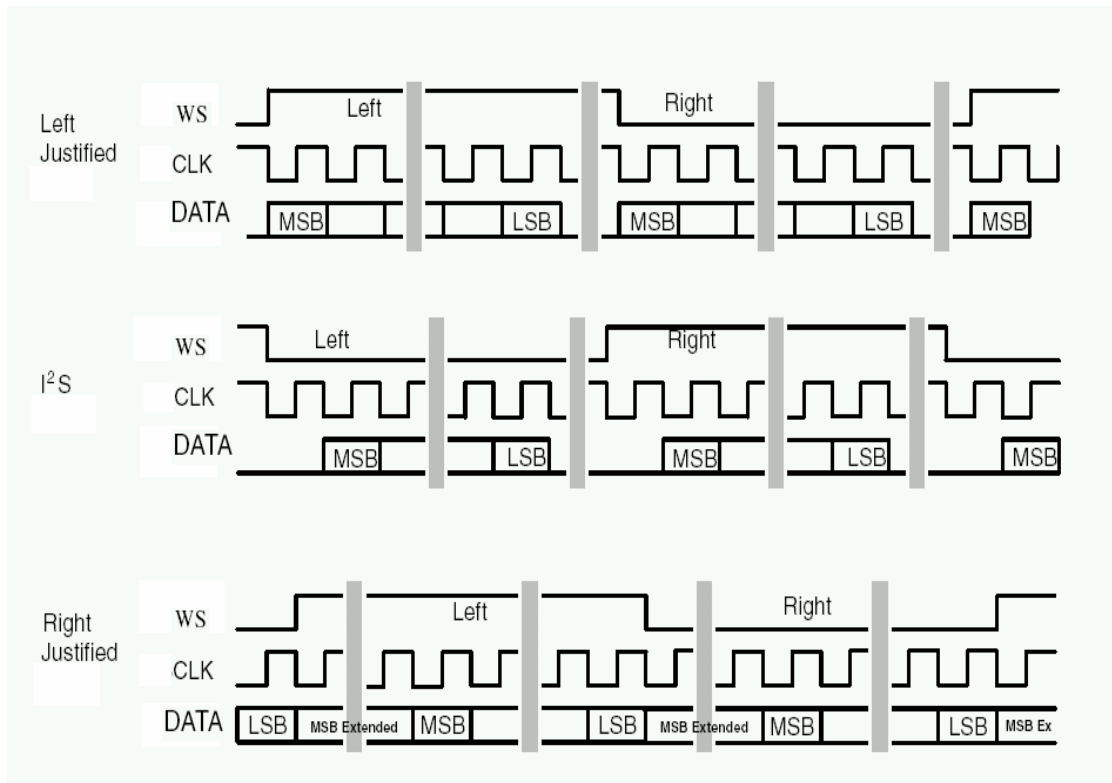


Figure 9-1 : nRF24Z1 package outline.



10 APPLICATION EXAMPLES

10.1 Ex. 1: Some I2S audio formats



I2S audio format	I2SCNF[3:0] value	Comment
Left justified	0xA	
I2S	0x0	
Right Justified	0xB	

Table 10-1 : Example of I2SCNF setting for some common audio formats



10.2 nRF24Z1 Application Scenarios

10.2.1 Notation :

ATX: nRF24Z1 audio transmitter

ARX: nRF24Z1 audio receiver

MCU: External microcontroller controlling nRF24Z1.

EEPROM: External EEPROM memory containing initial device set-up. Memory content is loaded during nRF24Z1 boot sequence.

Cinit: Initial nRF24Z1 register values hard coded in nRF24Z1, identical for all devices.

B_Einit: nRF24Z1 register broadcast values stored in EEPROM, these values are intended to be unique for a group of devices.

Einit: nRF24Z1 register values stored in EEPROM, these values are intended to be unique for a pair of ARX and ATX.

If no EEPROM memory is present at power on, Cinit values will apply to all registers, otherwise EEPROM values will be read and will override Cinit values.

Sreg: register values written to nRF24Z1 through ATX slave interface, these values will overwrite the values read from EEPROM.

Connect procedure: mode where two unknown ATX/ARX are paired, so that they thereafter will use identical register values read from their respective EEPROM or MCU.

10.2.2 Scenarios for controlling nRF24Z1

Scenario	connected to ATX	connected to ARX	Comment
A	nothing	nothing	Not planned to be used
B	EEPROM	nothing	ATX and ARX must link using Cinit values, and any nRF24Z1 will hence be able to link to any nRF24Z1 within radio range.
C	MCU	nothing	ATX and ARX must link using Cinit values, MCU can then write new Sreg to ATX, ATX will send over its Sreg values to ARX and a re-link will take place, see fig. 1.
D	nothing	EEPROM	Not planned to be used
E	EEPROM	EEPROM	Possible scenario : ATX and ARX will link using Einit values, see fig.2 and fig. 4. No connect procedure possible, see below ch 10.2.2.2
F	MCU	EEPROM	Primary scenario for nRF24Z1: ATX and ARX will link using Einit values, which may be set for instance during a connect procedure, see fig. 2. Connect procedure is described below in ch.10.2.2.1
G	nothing	MCU	Not planned to be used
H	EEPROM	MCU	Not planned to be used
I	MCU	MCU	Scenario much like F above. MCU on ARX side can interface nRF24Z1 and use it as a conduct to master controller at the ATX side.

Table 10-2 : nRF24Z1 application scenarios



10.2.2.1 Scenario F connect procedure

ATX side :

- MCU may read any ATX DD-input pin to act as a connect button to initiate this connect procedure
- MCU writes new ATX register values ADDR=B_Einit and CHP=B_Einit
- ATX will try to link
- When link is established, MCU writes ADDR=Sreg and CHP=Sreg to ARX EEPROM, and also sets ARX ADDR and CHP registers to Sreg values.
- MCU writes TXMOD7=0 to break link
- MCU writes ATX registers ADDR=Sreg and CHP=Sreg
- MCU writes TXMOD7=1 to establish new link
- Link will be established using Sreg values

ARX side:

- LNKM0D7 must be 1, otherwise ARX may not be taken over by an unknown ATX
- ARX will try to link using its Einit values, which will fail, assuming that its Einit partner is not within reach.
- ARX may then, if Connect-button is enabled and pushed, try to link using its B_Einit values, which will be successful.
- ARX will receive whatever ATX may send
- ARX will loose link when ATX establishes new link based on Sreg values.
- ARX will try to relink now using its new Sreg values, which are identical to the values used by ATX, so that the link will be successful. Note that Sreg values also have been written to ARX EEPROM by ATX, so that these values will be used whenever ARX is turned off and on.

10.2.2.2 Scenario E connect procedure

As seen for the connect procedure in scenario F, the MCU on ATX side must do things, and since in the E scenario there is no MCU, such a connect procedure is not possible. Both ATX and ARX will always use its Einit values when trying to establish a link. And the only way to change these values is to write new values directly to the respective EEPROMs. On the nRF24Z1 Evboard this is possible by connecting it to a PC and use the z1config PC software.



nRF24Z1 wireless audio streamer

Fig. 1: Scenario B or C

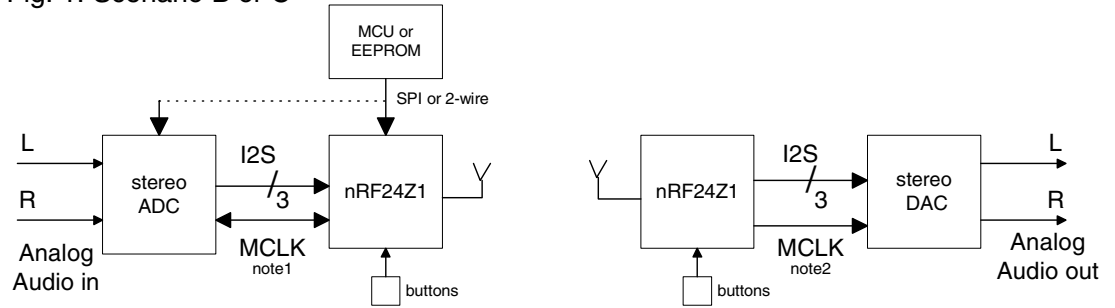


Fig. 2 : Scenario E or F

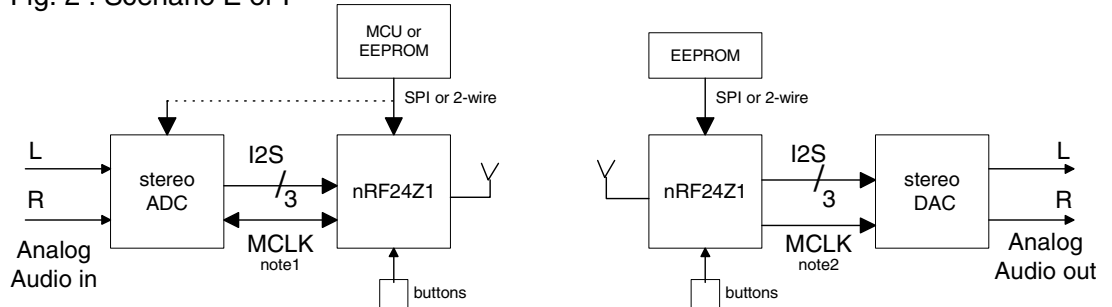


Fig. 3 : Scenario I

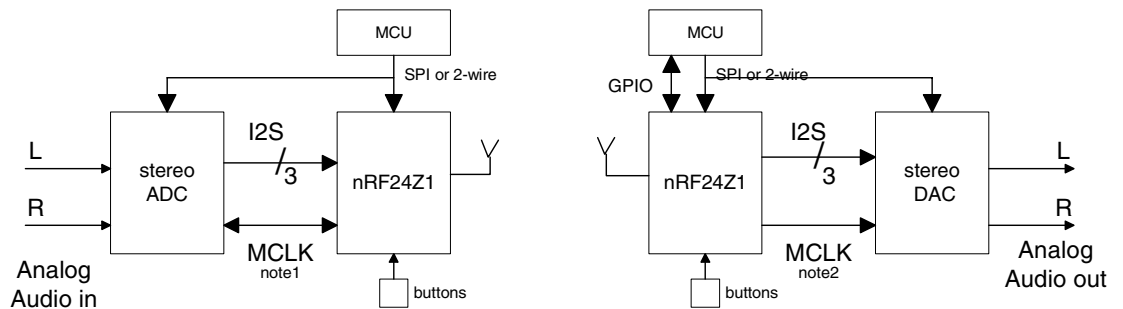
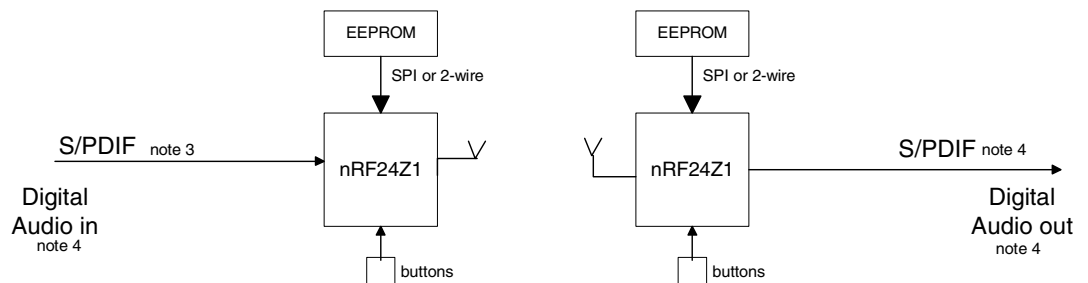


Fig. 4 : Scenario E with S/PDIF





nRF24Z1 wireless audio streamer

note 1 : MCLK may be either input to nRF24Z1, or generated by nRF24Z1, controlled by register TXMOD

note 2 : MCLK on audio receiver side is locked to MCLK on audio transmitter side

note 3 : S/PDIF input to nRF24Z1 is single ended CMOS level , and output from nRF24Z1 is full swing CMOS level, so some matching circuitry is necessary to connect to coax S/PDIF or optical S/PDIF.

- note 4 : it is also possible to have analog audio in and digital audio out and vice versa, or more precise all combinations of I2S or S/PDIF in and out are allowed, and audio out will be locked to audio in, regardless of audio format, as long as sampling rate in is within a range of +/- 500ppm of any of the supported sampling rates.



10.2.3 nRF24Z1 scenarios, examples from the EVBOARD

nRF24Z1-EVBOARD is equipped with EEPROM on both ATX and ARX side, and the table below describes how the scenarios described in Table 10-2 can be tested by using this evboard. Note that the EEPROM in addition to hold nRF24Z1 register values, also is used to store nRF24Z1 firmware. In this document only the register store function of the EEPROM is described. So that the meaning of "no EEPROM" is that the register storage function of EEPROM is missing. Naturally the firmware storage function is always there.

The z1config software running on a PC connected to the evboard via the J7 dongle port may be used both to set register values into EEPROM, and to load firmware into EEPROM.

10.2.4 Notation :

ETX : nRF24Z1-EVBOARD with nRF24Z1 audio transmitter

ERX : nRF24Z1-EVBOARD with nRF24Z1 audio receiver

Scenario (as described in Table 10-2)	Description
A	If EEPROM values are initialised to Cinit, the functional effect will be identical to a missing EEPROM, this applies to both ETX and ERX.
B	If ERX EEPROM values are initialised to Cinit, the functional effect will be identical to a missing EEPROM on ERX side
C	MCU function can be emulated by z1config software connected to ETX/J7 (dongle) port, or a MCU may be connected to ETX/JP5(SPI slave) or JP7(2-wire slave) port. If EEPROM values are initialised to Cinit, the functional effect will be identical to a missing EEPROM, this applies to both ETX and ERX.
E	default operation for evboard
F	MCU function can be emulated by z1config software connected to ETX/J7 (dongle) port, or a MCU may be connected to ETX/JP5(SPI slave) or JP7(2-wire slave) port. If ETX EEPROM values are initialised to Cinit, the functional effect will be identical to a missing EEPROM on ETX side
I	ETX MCU function can be emulated by z1config software connected to ETX/J7 (dongle) port, or a MCU may be connected to ETX/J5 (SPI slave) or JP7 (2-wire slave) port. ERX MCU can be connected to ERX/JP4 (SPI master) or JP6 (2-wire master) port. If EEPROM values are initialised to Cinit, the functional effect will be identical to a missing EEPROM, this applies to both ETX and ERX.

Table 10-3 : nRF24Z1-EVBOARD scenarios

Note: as nRF24Z1 evboard is equipped with a SPI EEPROM it is not possible to connect a 2-wire EEPROM to it as well, because the SPI EEPROM will be found first, as described in ch. 2.1



10.2.5 References

For latest version of documents, please visit <http://www.nordicsemi.no>

[1] nRF24Z1-EVB User Manual rev 1.2



11 ABSOLUTE MAXIMUM RATINGS

Supply Voltages

AVDD - 0.3V to + 3.6V

AVSS 0V

Input Voltage

V_I - 0.3V to AVDD + 0.3V

Output Voltage

V_O - 0.3V to AVDD + 0.3V

Total Power Dissipation

P_D ($T_A=85^\circ\text{C}$) 115mW

Temperatures

Operating temperature - 40°C to + 85°C

Storage temperature - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic sensitive device.

Observe precaution for handling.





12 GLOSSARY OF TERMS

Term	Description
ADC	Analog to Digital Converter
AM	Address Match
ARX	audio receiver
ATX	audio transmitter
CD	Carrier Detect
CHPA	SPI clock phase
CLK	Clock
CPOL	SPI clock polarity
CRC	Cyclic Redundancy Check
DR	Data Ready
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
LPCM	linear PCM (puls code modulation)
MBZ	Must Be Zero (reserved for future extensions)
MCU	Micro Controller Unit
RX	Receive
SPI	Serial Peripheral Interface
TX	Transmit
2-wire	2-wire serial interface compatible with I2C

Table 12-1 Glossary of terms nRF24Z1 family.



13 DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This datasheet contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 13-1. Definitions.

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic Semiconductor does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

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PRELIMINARY product specification revision date: 2005-03-18

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