Nordic VLSI ASA

nRF240x ShockBurst™ technology

1. Description of the ShockBurst™ technology

The nRF240x family from Nordic VLSI ASA has two different modes of operation, direct mode and ShockBurst™ mode. This document will describe the ShockBurst™ mode to clarify how the ShockBurst™ technology works and explain the advantages of its use.

The whole idea with the ShockBurst™ technology is to put as much low level protocol handling into the nRF chip as possible without removing any flexibility from the user.

2. ShockBurst™ advantages

2.1. Use of low cost micro-controllers

Even if the nRF240x devices uses a bit rate of 1Mbit/s on the air, is it possible for a low cost micro-controller to handle and operate a RF system based on these devices. A low cost micro-controller can look at the nRF240x device as a “advanced register” where data that shall be transmitted just has to be clocked in at a speed set by the micro-controller it self.
In receive mode it is even simpler, the micro-controller will be notified by the nRF2401 when a valid packet has arrived, and can then clock out the data at its own speed. In both cases there are no need for precise timing or high speed operation. This will give the user the possibility to utilise a low cost micro-controller with a internal RC oscillator, removing the need for an external crystal on the micro-controller.

Since the nRF2401 is doing all the low level protocol handling, like bit sampling, address checking and checksum calculation the micro-controller will not be loaded with this kind of work. This will again lead to the fact that the micro-controller can run on a even lower speed to perform its duties, making it possible to choose among the cheapest micro-controllers there is.

2.2. Low current consumption

Lets imagine that a micro-controller is limited to clock data in and out at a speed of 10kbit/s. Put this micro-controller in a design together with a transparent radio. Lets also imagine that this radio has a current consumption of 8mA when transmitting. Lets then calculate the energy per transmitted bit that this system uses:
8mA/10kbit/s=0.8uAs/bit.

Lets then look at the same micro-controller used together with a nRF240x device in ShockBurst™ mode: The nRF240x has a speed of 1Mbit/s on air. Since the nRF240x stays in sleep mode when the packet is clocked into its Data Out Register, it will only use current when transmitting the packet. The nRF240x device uses 8mA in transmit mode, but since the bit rate on air is 1Mbit/s it will use only 8mA/1Mbit/s=8nAs/bit, that is 1/100 times the energy used by the first design. This means that the design with the nRF240x device will be able to use a given battery 100 times longer than the other design, transmitting the same amount of data.

In addition to the fact that the nRF240x will use very little energy per transmitted bit, current will also be saved due to the fact that the micro-controller can hibernate when the nRF240x is receiving or transmitting data. This is not possible without the ShockBurst™ technology.

2.3. Very low system cost

Since the ShockBurst™ technology makes it possible to use a low cost micro-controller with just a internal RC oscillator, the need for external components around the micro-controller will be kept to a minimum. The nRF240x it self has also very few external components, so the total bill of material will be extremely low. The low energy per transmitted bit will open for use of less expensive battery technology.

3. Physical connection

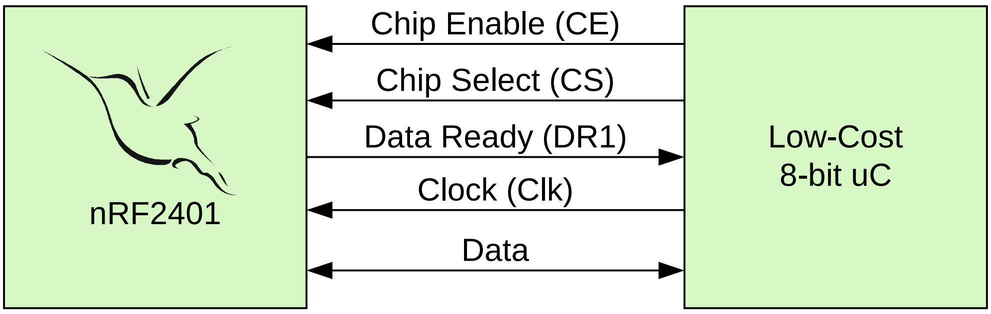

Figure 1: Physical connection of a nRF2401 and a low-cost uC.

A micro-controller that is going to operate the nRF2401 in ShockBurst™ mode has to use five general I/O pins for interfacing the nRF2401. The five signals it has to operate are shown in Figure 1. A more detailed description of how to use these signals can be found in the nRF2401 data sheet.

Before operating the nRF240x in ShockBurst™ mode, it has to be configured. Please refer to the nRF2401 data sheet for description on how this is done.

4. The ShockBurst™ technology, transmit mode

Inside the nRF2401 we have the ShockBurst Engine (SBE.)

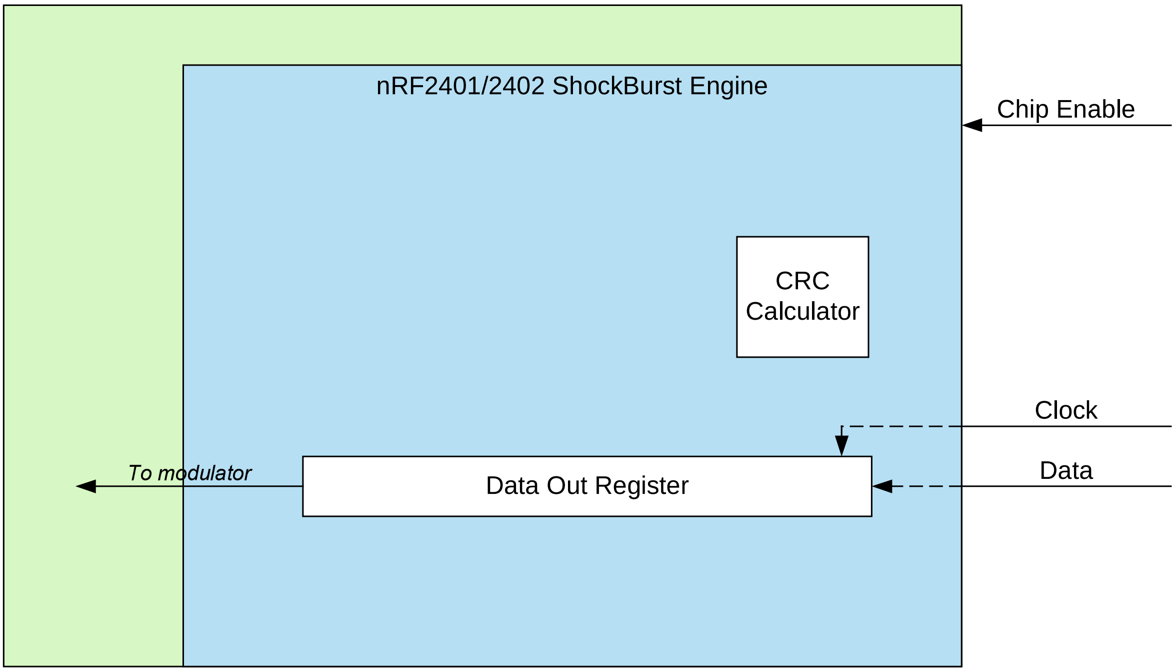

Figure 2: The ShockBurst Engine in transmit mode.

In transmit mode the ShockBurst Engine works like this:

1. The external low cost micro-controller will first of all configure the nRF device to use the right channel, output power and if it is going to use Cyclic Redundant Check (CRC) or not.
2. The micro-controller decides that it will transmit a packet via the nRF240x device, and pulls the Chip Enable signal high.
3. The micro-controller clocks its packet into the Data Out Register, using the Clock and Data pin on the nRF240x. The packet contains receivers address and the payload.
4. If CRC is enabled, the SBE will calculate the CRC of the data that is being clocked in, and the result will be attached to the transmitted packet.

5. Transmission of the packet will start 202us after the Chip Enable signal has been pulled low by the micro-controller.

5. The ShockBurst™ technology, receive mode

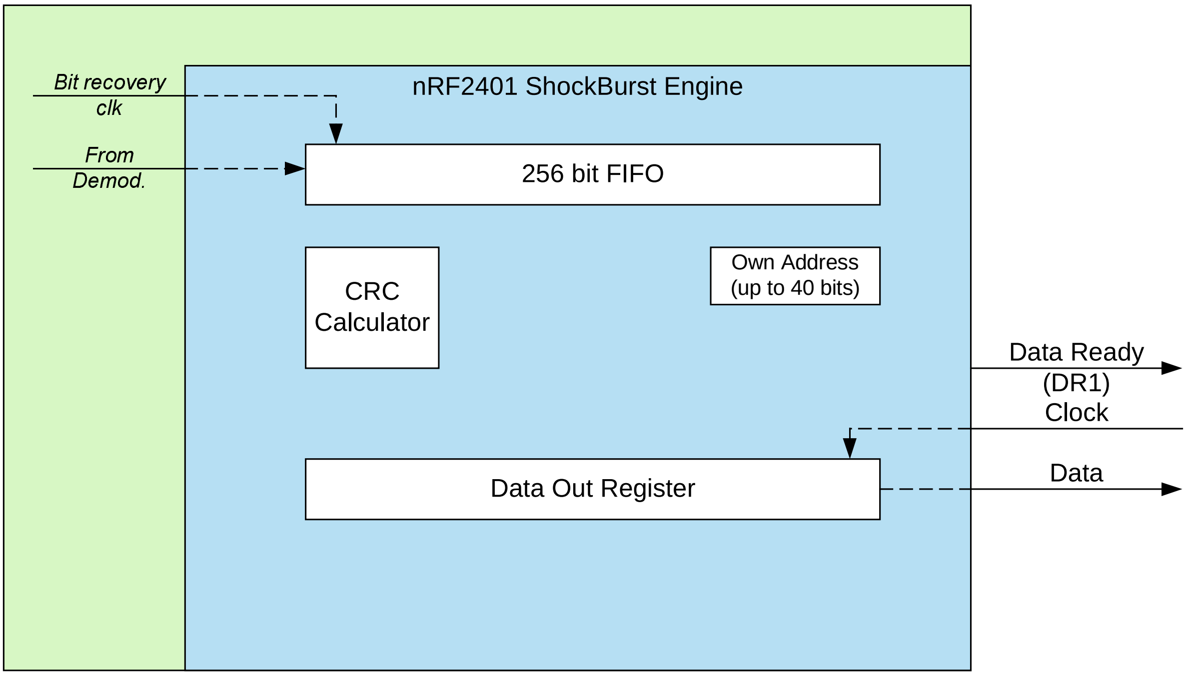

Figure 3: The ShockBurst Engine in receive mode

This is how the ShockBurst Engine works in receive mode:

1. The external low cost micro-controller will before operation configure the nRF2401. During this configuration the nRF2401 will be told what is its own address, what packet length it shall receive, what bit rate (250kbit/s or 1Mbit/s) it shall use on air and if it shall perform CRC or not. In this case we assume that own address is N bits wide, the packet is P long and it shall perform CRC. After configuration of the nRF2401, the low cost micro-controller can go into hibernation.
2. At this moment a transmitter starts to transmit a packet to this receiver.
3. From the nRF2401 demodulator the bits are clocked into a 256 bit wide First In First Out (FIFO) register at the same bit rate that is used on air.
4. Every time a new bit is clocked into the FIFO register from the demodulator, the N first bits in the FIFO will be compared with own address.
5. If the bits match the CRC calculator will calculate the checksum of the whole packet and compare if the result is equal to the CRC bits in the received packet. If the CRC does not match, the SBE will continue to compare incoming bits with own address until a new match is found, and then repeat the CRC calculation.
6. If both address and CRC match, the payload part of the packet, that is the whole packet except the N address bits and the CRC bits, will be copied into the Data Out Register. At the same time the Data Ready (DR1) signal will be set high.
7. The external low cost micro-controller with the DR1 signal connected to one of its interrupt I/O pins can now wake up from its hibernating state, knowing that a new packet of data has arrived.
8. The micro-controller can now generate a clock signal on the clock pin on the nRF2401, and the received payload will be clocked out from the Data Out Register. When the whole payload is clocked out, the DR1 signal will go low. The

low cost micro-controller can do this clocking at its own speed making it possible to use a micro-controller with a slow internal RC oscillator.

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