AL9V576
MPEG-4/2/1 A/V Encoder
Datasheets

Version 1.0

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Amendments

2006.5.19 Formal release version 1.0

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1. General Description

AL9V576 is a real-time MPEG-4/2/1 video/audio encoder chip that fully complies with ISO/IEC-11172, ISO/IEC-13818, and ISO/IEC-14496 standard. The video encoder accepts raw ITU-R BT.656, ITU-R BT.601, or 16-bit YCbCr video and compresses the video into MPEG-4/2/1 formats. The audio encoder accepts the digital audio and compresses the audio into MPEG-1 Layer-2 audio formats. AL9V576 multiplexes the video and audio streams as transport streams for communication applications or program streams for storage applications.

2. Features

The following lists the main features of the AL9V576 MPEG-4/2/1 video/audio encoder.

Video Encoder

- High quality real-time MPEG-1, MPEG-2 MP@ML, and MPEG-4 ASP encoding
- Variable frame rate up to 30fps for NTSC or 25fps for PAL
- Variable resolution up to full D1
- Internal vertical and horizontal scaling down filters
- Variable or constant bit rate (VBR/CBR)
- YUV 4:2:2 to 4:2:0 conversion
- Adaptive rate control and adaptive quantization algorithms
- Scene change detection
- Programmable GOP structure: I, IP, IBP, IBBP
- Automatic 3:2 pull-down detection
- Large motion estimation search window:
  - X: +/- 120 pixels; Y: +/- 80 pixels for P frame
  - X: +/- 80 pixels; Y: +/- 60 pixels for B frame
- Half-pel accuracy
- Frame or field motion estimation
- High quality video pre-processing: both temporal and spatial filtering
- Motion estimation assisted TBC
- Speckle noise reduction
- Recursive noise reduction
- Horizontal/Vertical cropping
- Intelligent exception handling mechanism allows stably encoding for various video input conditions

Audio Encoder

- MPEG-1 layer II encoding with psychoacoustic model
- Variable sampling rate supported: 32K, 44.1K, 48K Hz.
- Variable bit rate up to 384Kbps

System Multiplexing and De-Multiplexing

- Multiplexing of video and audio streams according to ISO13818-1 MPEG-2 systems standard
- Video Elementary Stream (ES) and Packetized Elementary Stream (PES) format
- MPEG-1 System and VCD Stream format.
- MPEG-2 Program Stream (PS), Transport Stream (TS) and DVD formats
- MPEG-4 elementary stream and AVI format
- MPEG-4 video embedded in MPEG-2 PS or TS format
- MPEG time stamp (PTS/DTS/SCR/PCR) generation and insertion
- Insertion of user data in the GOP header or in the picture header
- Insertion of Closed Caption data

Peripheral Interface

- Video Input:
  - Digital video input: 8-bit YUV 4:2:2 supports ITU-R BT.656 format or 16-bit YUV 4:2:2 supports ITU-R BT.601 format
- Audio Input:
  - Digital audio input: Left-Justified slave mode
- Host Interface:
  - 8/16-bit Intel-style host interface
  - 32-bit PCI (33MHz) interface (256-TfBGA only)
  - 8/16-bit SRAM-like host interface
- System Interface:
  - 1/8-bit encoded bit stream output
  - Max. 12 Multi-function IO pins
  - 2-Wire Serial bus (master mode)

Others

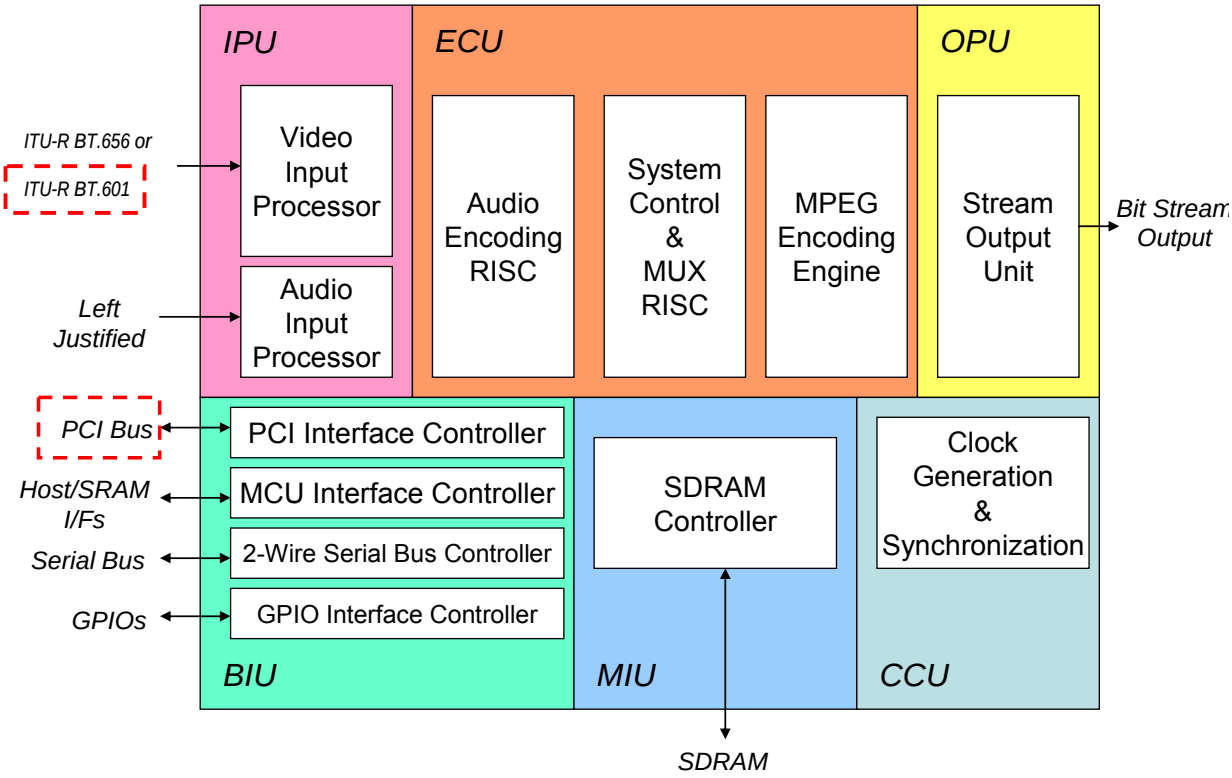
- Core voltage: 1.8V
- I/O voltage: 3.3V
- Packages: TfBGA-256 & LQFP-160

3. Applications

- PCI MPEG-4/2 A/V capture card
- USB2.0 MPEG-4/2 A/V TV box
- DVR cards/Surveillance PCI capture card (Multiple-channel)
- IP camera
- Video server
- Surveillance DVR
- DVD Recorder
- PVR/PMP
- MPEG-4 viewer
- Digital AV sender
- Wireless TV
- Network video phone, etc.

4. Function Block Diagram

AL9V576 chip is an MPEG-4/2/1 video/audio encoder. Figure 4.1 shows the function block diagram of AL9V576 chip.



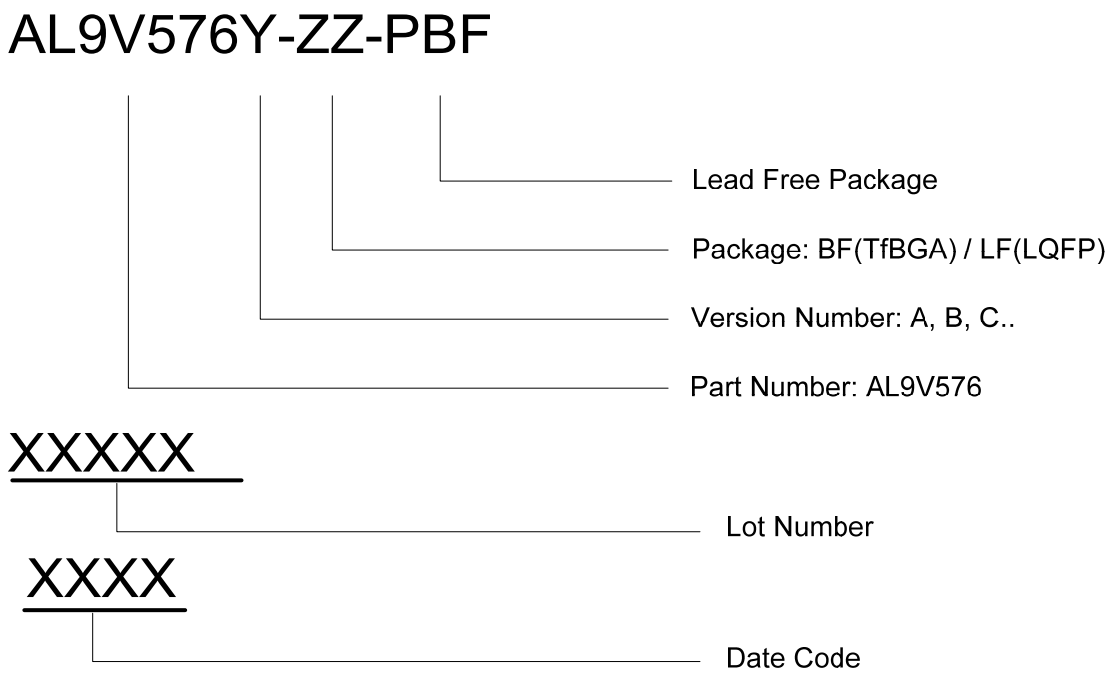
Note: The red-colored notations are only for TfBGA-256 package.

Figure 4.1: AL9V576 block diagram

There are two RISC Processors in AL9V576. The "System Control & MUX RISC Processor" is responsible for the control of video encoding and bit stream multiplexing. The "Audio Encoding RISC Processor" processes the audio encoding. The Video Input Processor is responsible for several input pre-processing functions: color space conversion, scaling down of video resolution, synchronization detection, and noise reduction filtering. The Audio Input Processor receives audio in Left-Justified format and organizes the data before storing it in SDRAM. The video compression is handled by the MPEG Encoding Engine. The MCU Interface controller provides an interface between AL9V576 and the general-purpose microcontroller. The 2-Wire Serial Bus Controller provides AL9V576 another mechanism to communicate with other components on the system. The Memory Controller generates the addresses and the control signals to access the external SDRAM. AL9V576 also supports PCI interface as an alternative for the host to access the memory and registers of AL9V576.

5. Chip Information

5.1 Marking Information



5.2 Order Information

AL9V576 is available in 256-pin TFBGA and 160-pin LQFP packages.

Part number	Package	Power Supply
AL9V576B-BF-PBF	TfBGA 256-pin (14mm x 14mm x 1.2mm)	+1.8/3.3V
AL9V576B-LF-PBF	LQFP 160-pin (20mm x 20mm x 1.4mm)	+1.8/3.3V

Note: AverLogic Technologies Pb-Free products employ special Pb-Free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish do not use materials containing PBB, PBDE or red phosphorus for green-product chips. AverLogic's Pb-Free products are MSL classified at Pb-Free peak reflow temperatures that meet or exceed the Pb-Free requirements of IPC/JEDEC J Std-020C."

6. Pin Description and Configuration

6.1. Introduction

AL9V576 comes with two types of packages. The TfBGA 256-pin package (AL9V576-BF256) is used for AL9V576 with full feature set, and LQFP 160-pin package (AL9V576-LF160) is used as an economical version that supports only partial of the feature set.

6.2. Pin Definition for AL9V576 with TfBGA-256 Package

Table 6.2.1: List of Pins for AL9V576 with TfBGA-256 package

Pin Name	Pin Number	I/O Type	Description
RST_N	R12	I	System reset
UP_SEL	K7	I	Microcontroller interface mode select Low: Intel-style High: SRAM-like
UP_AD[15:0]	N10,M10,M9,N9, L9,L8,N8,M8,L7, N7,M7,M6,L6,K5, M5,L5	I/O	Microcontroller interface address/data port [15:0]
UP_RDY_N	N11	O	Microcontroller interface ready signal Intel-style: Low active SRAM-like: High active
UP_RD_N	P11	I	Microcontroller interface read enable Intel-style: Low active SRAM-like: High active
UP_WR_N	L10	I	Microcontroller interface write enable Intel-style: Low active SRAM-like: High active
UP_ALE/ H_ADDR[0]	P12	I	Microcontroller interface address latch enable or SRAM interface address bit 0 Intel-style: Low active
UP_CS_N	M11	I	Microcontroller interface chip select Intel-style: Low active SRAM-like: High active

Pin Name	Pin Number	I/O Type	Description
H_ADDR[1]	N12	I	SRAM interface address
H_ADDR[2]	T13	I	SRAM interface address
H_ADDR[3]	R13	I	SRAM interface address
AD[31:0]	N2,T1,P1,R1,T2, R2,P2,P3,R3,R4, T4,P4,N4,R5,T5, P5,R8,T9,R9,P9, T10,R10,P10,N14, P16,T15,R15,T16, N16,R16,N15,P15	I/O	PCI AD signals [31:0]
CBE[3:0]	T3,N5,P8,P14	I	PCI CBE signals [3:0]
PAR	P7	I/O	PCI PAR signal
FRAME_N	R6	I	PCI FRAME signal
IRDY_N	T6	I	PCI IRDY signal
TRDY_N	P6	O	PCI TRDY signal
STOP_N	T7	O	PCI STOP signal
DEVSEL_N	N6	O	PCI DEVSEL signal
PERR_N	R7	O	PCI PERR signal
IDSEL	N3	I	PCI IDSEL signal
PCI_RST_N	M4	I	PCI reset
PCLK	N1	I	PCI clock
PCI_HOST	R11	I	Select PCI or microcontroller mode Low: Microcontroller High: PCI
EEDI	L13	I	EEPROM port (to EEPROM data output)
EEDO	L15	O	EEPROM port (to EEPROM data input)
EECK	M15	O	EEPROM port
STR_CLK	H16	I/O	Encoded bit stream output clock
STR_DREQ_N	J15	I	Encoded bit stream data request
STR_GNT	H15	I	Encoded bit stream data bus grant: Low active
STR_DVLD_N	H14	I/O	Encoded bit stream data valid
STR_OTP	J16	O	Encoded transport stream
STR_DATA[7:0]	D14,E14,F15,F16,	O	Encoded bit stream output [7:0]

Pin Name	Pin Number	I/O Type	Description
	F14,G15,G16,G14		
SDA	E15	I/O	2-wire serial bus data line
SCL	E16	I/O	2-wire serial bus clock line
GPIO[1:0]	L14,T8	I/O	GPIOS (GPIO[1:0] can not be used for interrupt.)
GPIO[11:2]	K15,K16,K14,K6, R14,L16,N13,P13, M13,M14	I/O	GPIO
BIST_MODE	J14	I	BIST mode (Tied to low)
A_CLK	A7	I	Audio input clock
A_LEFT	C7	I	Audio left/right channel select
A_DATA	D7	I	Audio data input
TEST_MODE	C14	I	Test mode (Tied to low)
VID_CLK	A16	I	Video input clock
VIDEO_D0[7:0]	D16,D15,C16,B16, C15,A15,B15,B14	I	BT656 video input
CLK_27	A14	I	27 MHz clock input for time stamp
SDR_DQ[31:0]	B7,C6,D6,A6,B6, B5,C5,A5,B1,A1, A2,B3,A3,B4,A4, D5,B2,C2,C4,C1, C3,D2,D4,D1,F2, F1,F3,E3,E1,E4, E2,D3	I/O	SDRAM data [31:0]
SDR_ADDR[10: 0]	J2,M3,M1,L3,L1, L4,L2,K4,K1,K3, K2	O	SDRAM address [10:0]
SDR_BA[1:0]	J1,J4	O	SDRAM bank address
SDR_CKE	H3	O	SDRAM clock enable
SDR_CS_N	J3	O	SDRAM chip select
SDR_RAS_N	H2	O	SDRAM command
SDR_CAS_N	H1	O	SDRAM command
SDR_WE_N	H4	O	SDRAM command
SDR_DQM[3:0]	F4,G4,G3,G2	O	SDRAM input/output mask

Pin Name	Pin Number	I/O Type	Description
SDR_CLK_OUT	G1	O	SDRAM clock out
SDR_CLK_IN	T11	I	SDRAM clock in
PLL_CIN	M16	I	PLL reference clock input or bypassed clock
VDD2_1.8	E6,E8,E10,E12,F5, F13,G13,H5,H12, J13,K8,K13,M12, L11	P	Digital Power 1.8V
PLL_VCC18A	T14	P	PLL Analog Power 1.8V
VDD3_3.3	E5,E7,E9,E11,E13, F12,G5,G12,H13, J5,J12,K9,K12	P	Digital Power 3.3V

GND	F6,F7,F8,F9,F10, F11,G6,G7,G8,G9, G11,H6,H7,H8,H9, H10,H11,J6,J7,J8, J9,J10,J11,K10, K11,L12		Digital Ground
PLL_GND18A	T12		PLL Analog Ground

Figure 6.2.2 Top-view pin location for AL9V576 with TfBGA-256 package

Coordinate	1	2	3	4	5	6	7	8
A	SDR_DQ[22]	SDR_DQ[21]	SDR_DQ[19]	SDR_DQ[17]	SDR_DQ[24]	SDR_DQ[28]	A_CLK	VIDEO_D1[1]
B	SDR_DQ[23]	SDR_DQ[15]	SDR_DQ[20]	SDR_DQ[18]	SDR_DQ[26]	SDR_DQ[27]	SDR_DQ[31]	VIDEO_D1[0]
C	SDR_DQ[12]	SDR_DQ[14]	SDR_DQ[11]	SDR_DQ[13]	SDR_DQ[25]	SDR_DQ[30]	A_LEFT	VIDEO_D1[3]
D	SDR_DQ[8]	SDR_DQ[10]	SDR_DQ[0]	SDR_DQ[9]	SDR_DQ[16]	SDR_DQ[29]	A_DATA	VIDEO_D1[2]
E	SDR_DQ[3]	SDR_DQ[1]	SDR_DQ[4]	SDR_DQ[2]	VDD3_3.3	VDD2_1.8	VDD3_3.3	VDD2_1.8
F	SDR_DQ[6]	SDR_DQ[7]	SDR_DQ[5]	SDR_DQM[3]	VDD2_1.8	GND	GND	GND
G	SDR_CLK_OUT	SDR_DQM[0]	SDR_DQM[1]	SDR_DQM[2]	VDD3_3.3	GND	GND	GND
H	SDR_CAS_N	SDR_RAS_N	SDR_CKE	SDR_WE_N	VDD2_1.8	GND	GND	GND
J	SDR_BA[1]	SDR_ADDR[10]	SDR_CS_N	SDR_BA[0]	VDD3_3.3	GND	GND	GND
K	SDR_ADDR[2]	SDR_ADDR[0]	SDR_ADDR[1]	SDR_ADDR[3]	UP_AD[2]	GPIO[8]	UP_SEL	VDD2_1.8
L	SDR_ADDR[6]	SDR_ADDR[4]	SDR_ADDR[7]	SDR_ADDR[5]	UP_AD[0]	UP_AD[3]	UP_AD[7]	UP_AD[10]
M	SDR_ADDR[8]	NC	SDR_ADDR[9]	PCI_RST_N	UP_AD[1]	UP_AD[4]	UP_AD[5]	UP_AD[8]
N	PCLK	AD[31]	IDSEL	AD[19]	CBE[2]	DEVSEL_N	UP_AD[6]	UP_AD[9]
P	AD[29]	AD[25]	AD[24]	AD[20]	AD[16]	TRDY_N	PAR	CBE[1]
R	AD[28]	AD[26]	AD[23]	AD[22]	AD[18]	FRAME_N	PERR_N	AD[15]
T	AD[30]	AD[27]	CBE[3]	AD[21]	AD[17]	IRDY_N	STOP_N	GPIO[0]
Coordinate	1	2	3	4	5	6	7	8

9	10	11	12	13	14	15	16	Coordinate
VIDEO_D1[5]	VIDEO_D2[1]	VIDEO_D2[5]	VS1	FID	CLK_27	VIDEO_D0[2]	VID_CLK	A
VIDEO_D1[4]	VIDEO_D2[0]	VIDEO_D2[4]	HS1	DE	VIDEO_D0[0]	VIDEO_D0[1]	VIDEO_D0[4]	B
VIDEO_D1[7]	VIDEO_D2[3]	VIDEO_D2[7]	VS2	COAST	TEST_MODE	VIDEO_D0[3]	VIDEO_D0[5]	C
VIDEO_D1[6]	VIDEO_D2[2]	VIDEO_D2[6]	HS2	CSYNC	STR_DATA[7]	VIDEO_D0[6]	VIDEO_D0[7]	D
VDD3_3.3	VDD2_1.8	VDD3_3.3	VDD2_1.8	VDD3_3.3	STR_DATA[6]	SDA	SCL	E
GND	GND	GND	VDD3_3.3	VDD2_1.8	STR_DATA[3]	STR_DATA[5]	STR_DATA[4]	F
GND	GND	GND	VDD3_3.3	VDD2_1.8	STR_DATA[0]	STR_DATA[2]	STR_DATA[1]	G
GND	GND	GND	VDD2_1.8	VDD3_3.3	STR_DVLD_N	STR_GNT	STR_CLK	H
GND	GND	GND	VDD3_3.3	VDD2_1.8	BIST_MODE	STR_DREQ_N	STR_OTP	J
VDD3_3.3	GND	GND	VDD3_3.3	VDD2_1.8	GPIO[9]	GPIO[11]	GPIO[10]	K
UP_AD[11]	UP_WR_N	VDD2_1.8	GND	EEDI	GPIO[1]	EEDO	GPIO[6]	L
UP_AD[13]	UP_AD[14]	UP_CS_N	VDD2_1.8	GPIO[3]	GPIO[2]	EECK	PLL_CIN	M
UP_AD[12]	UP_AD[15]	UP_RDY_N	H_ADDR[1]	GPIO[5]	AD[8]	AD[1]	AD[3]	N
AD[12]	AD[9]	UP_RD_N	UP_ALE	GPIO[4]	CBE[0]	AD[0]	AD[7]	P
AD[13]	AD[10]	PCI_HOST	RST_N	H_ADDR[3]	GPIO[7]	AD[5]	AD[2]	R
AD[14]	AD[11]	SDR_CLK_IN	PLL_GND18A	H_ADDR[2]	PLL_VCC18A	AD[6]	AD[4]	T
9	10	11	12	13	14	15	16	Coordinate

6.3. Pin Definition for AL9V576 with LQFP-160 Package

Table 6.3.1 Pin list for AL9V576 with LQFP-160 package

Pin Name	Pin Number	I/O Type	Description
RST_N	41	I	System reset
UP_SEL	42	I	Microcontroller interface mode select Low: Intel-style High: SRAM-like
UP_AD[15:0]	63,62,61,60, 59,56,55,54, 53,52,51,48, 47,46,45,44	I/O	Microcontroller interface address/data port [15:0]
UP_RDY_N	68	O	Microcontroller interface ready signal Intel-style: Low active SRAM-like: High active
UP_RD_N	67	I	Microcontroller interface read enable Intel-style: Low active SRAM-like: High active
UP_WR_N	64	I	Microcontroller interface write enable Intel-style: Low active SRAM-like: High active
UP_ALE	71	I	Microcontroller interface address latch enable or SRAM interface address bit 0 Intel-style: Low active
UP_CS_N	69	I	Microcontroller interface chip select Intel-style: Low active SRAM-like: High active
H_ADDR[3:1]	74,73,72	I	SRAM interface address [3:1]
STR_CLK	96	I/O	Encoded bit stream output clock
STR_DREQ_N	93	I	Encoded bit stream data request
STR_GNT	94	I	Encoded bit stream data bus grant: Low active

Pin Name	Pin Number	I/O Type	Description
STR_DVLD_N	95	I/O	Encoded bit stream data valid
STR_OTP	92	O	Encoded transport stream
STR_DATA[7:0]	106,105,104, 103,102,101, 100,97	O	Encoded bit stream output [7:0]
SDA	110	I/O	2-wire serial bus data line
SCL	107	I/O	2-wire serial bus clock line
GPIO[11:2]	90,89,88,43, 85,84,83,82, 80,79	I/O	GPIO [11:2]
BIST_MODE	91	I	BIST mode (Tied to low)
A_CLK	129	I	Audio input clock
A_LEFT	130	I	Audio left/right channel select
A_DATA	133	I	Audio data input
VID_CLK	123	I	Video input clock
VIDEO_D0[7:0]	111,112,113, 114,115,116, 117,120	I	BT656 video input
CLK_27	124	I	27 MHz clock input for time stamp
SDR_DQ[31:0]	134,135,136, 137,138,139, 140,143,144, 145,146,147, 148,149,150, 153,154,155, 156,157,158, 159,160,1,2,3, 4,5,6,7,8,11	I/O	SDRAM data [31:0]
SDR_ADDR[10:0]	38,37,36,35, 34,33,32,31, 28,27,26	O	SDRAM address [10:0]
SDR_BA[1:0]	21,18	O	SDRAM bank address [1:0]
SDR_CKE	17	O	SDRAM clock enable
SDR_CS_N	16	O	SDRAM chip select

Pin Name	Pin Number	I/O Type	Description
SDR_RAS_N	15	O	SDRAM command
SDR_CAS_N	14	O	SDRAM command
SDR_WE_N	13	O	SDRAM command
SDR_DQM[3:0]	22,23,24,25	O	SDRAM input/output mask [3:0]
SDR_CLK_OUT	12	O	SDRAM clock out
SDR_CLK_IN	70	I	SDRAM clock in
PLL_CIN	81	I	PLL reference clock input or bypassed clock
VDD2_1.8	20,40,50,65, 98,119,131,151	P	Digital Power 1.8V
PLL_VCC18A	86	P	PLL Analog Power 1.8V
VDD3_3.3	19,39,49,66, 99,118,132, 152	P	Digital Power 3.3V
GND	9,10,29,30,57, 58,75,76,108, 109,125,126, 127,128,141, 142	P	Digital Ground
PLL_GND18A	78	P	PLL Analog Ground
Reserved pin	77	P	Suggest link to PLL Analog Power 1.8V
Reserved pin	87	P	Suggest link to PLL Analog Ground
NC	121,122		

6.4. Pin Configuration for AL9V576 with LQFP-160 Package

Figure 6.4.1 shows the top-down pin location view of AL9V576 with LQFP-160 package.

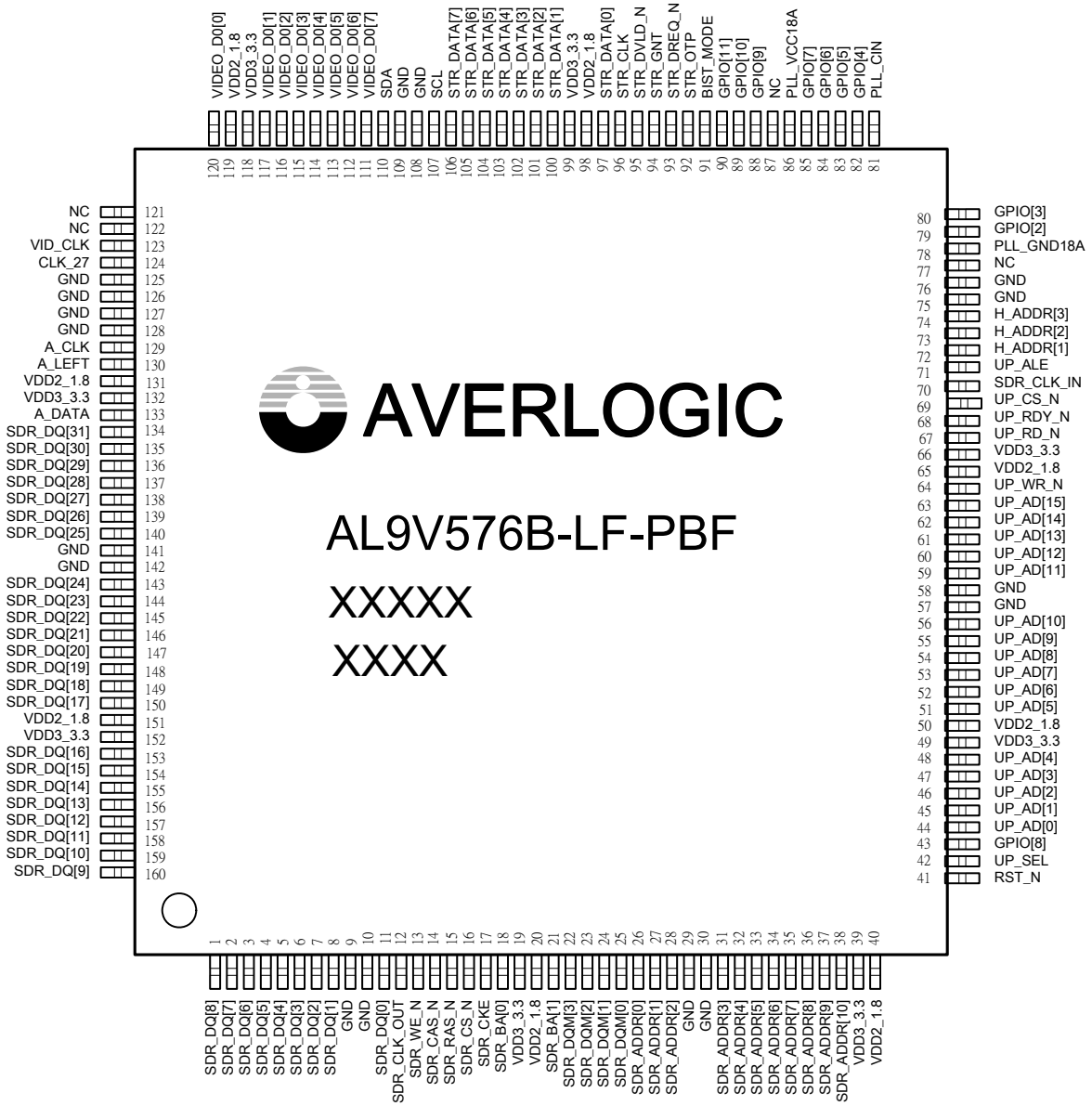


Figure 6.4.1: Top-down pin location view for AL9V576 with LQFP-160 package

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

(Exceeding the rating can be harmful to product life. These are only user guidelines and are not tested.)

Parameter			Rating	Unit
V_{CC-1}	Supply Voltage-1.8V		N/A	V
V_{CC-2}	Supply Voltage-3.3V		-0.5 ~ +3.6	V
V_P	Input Pin Voltage		-0.5 ~ +3.6	V
I_O	Output Current		-20 ~ +20	mA
T_{stg}	Storage Temperature		-40 ~ +125	°C
T_{VSOL}	Vapor Phase Soldering Temperature (15 Sec.)	Without PBF	220	°C
		With PBF	260	

7.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Unit
V_{CC-1}	Supply Voltage	1.71	1.8	1.89	V
V_{CC-2}	Supply Voltage	3.15	3.3	3.45	V
T_{AMB-2}	Ambient Operation Temperature	0	-	70	°C

7.3. DC Characteristics

(3.3V, GND=0V, T_{AMB} = 0 to 70°C)

Parameter		Min.	Typ.	Max.	Unit
V_{IH}	Hi-level Input Voltage	2.0		3.6	V
V_{IL}	Low-level Input Voltage	0		0.8	V
C_{IN}	Input Capacitance		4	5	pF
I_{IL}	Input Leakage Current (V_{CC} = 3.6V, V_{IN} = 0V)	-10			μA
I_{IH}	Input Leakage Current (V_{CC} = 3.6V, V_{IN} = 3.6V)			10	μA
V_{OH}	Output Logic '1' Voltage, I_{OH}=-4mA	2.4			V
V_{OL}	Output Logic '0' Voltage, I_{OL}=4mA			0.5	V
I_{CC-1}	Dynamic Operating Current (1.8V, 133MHz)		550		mA
I_{CC-2}	Dynamic Operating Current (3.3V, 133MHz)		20		mA

8. Peripheral Interface Descriptions

The peripheral interfaces of AL9V576 include:

Video Input Interface
Audio Input Interface
PCI Target Interface (TfBGA-256 only)
Host Interface
- ✓ 8-bit 8051 Host Interface
- ✓ 8/16-bit 8051 (Intel-style) Host Interface
- ✓ 8/16-bit SRAM-Style Microcontroller Interface

System Interface
- ✓ 1/8-bit Encoded Bit Stream Output Interface
- ✓ GPIO Interface
- ✓ 2-Wire Serial Bus (I^2C-like) Interface

Each of interfaces above is illustrated as follows.

8.1. Video Input Interface

AL9V576 provides an 8-bit ITU-R BT.656 video input interface to connect to various video input signals. The function of the Video Input Processor can be divided into two blocks, Sync Processor and Video Pipeline. Sync Processor detects the type of input source and regenerates internal V-sync, H-sync, and Data Enable signals to control Video Pipeline. Video Pipeline is the data-path for video processing which consists of offset adjustment and image down-scaling. The scaling down function is capable of reducing the image resolution to any ratio in both vertical and horizontal directions. The bandwidth of the encoder is limited to 720x480 at 30 frames per second or 720x240 at 60 fields per second; therefore, video sources with larger resolution have to be scaled down before input to the encoder.

Table 8.1.1 lists the video input formats supported by AL9V576.

Table 8.1.1 Video Input Configuration

Input Format	Total Bits	Sampling	Input Video
ITU-R BT.656	8	4:2:2	YCbCr
			YCrCb

Figure 8.1.1 shows the timing and format of ITU-R BT.656 input video. Figure 8.1.2 shows the timing constraints of ITU-R BT.656 input data with respect to the 27 MHz sampling clock.

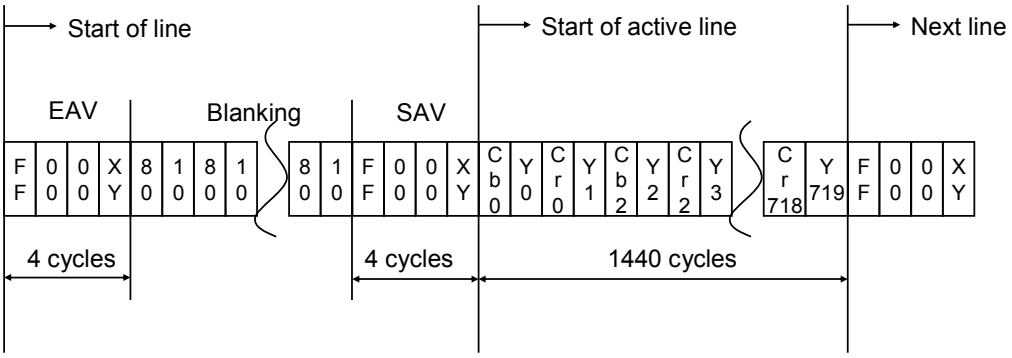
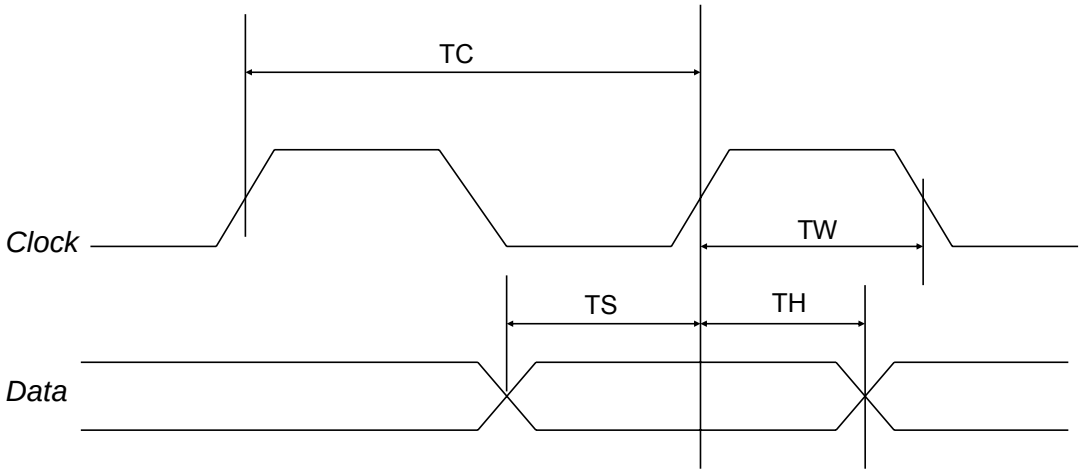


Figure 8.1.1: ITU-R BT.656 data format and timing



TW = 18.5 ± 3 ns
TC = 37 ns
TS ≥ 5 ns
TH ≥ 3 ns

Figure 8.1.2: ITU-R BT.656 video input timing constraints

To enhance the capability of video capturing, AL9V576 is designed with the following functions:

1. Source detection: The Video Input Processor of AL9V576 constantly monitors the length between tow Hsync signals and the number of lines between two consecutive Vsync signals. When changes detected, the video input processor triggers an interrupt service routine in the RISC processor to handle the source change.
2. Active window capture: AL9V576 generates the internal data enable signal to mask the active video data in both horizontal and vertical directions. This function can also be used to crop the image size. The capture window is set by programming the “HSTART”, “HLENGTH”, “VSTART”, and “VLENGTH” registers. Figure 8.1.4 illustrates the timing of video capture.

3. Sync generation: AL9V576 can re-generate the clean Sync signals for the internal datapath by detecting the polarity and the length of external Hsync, Vsync, or Csync signals.
4. Scaling: AL9V576 uses a 9-bit scaling factor for image scaling down in both horizontal and vertical directions. The output image size will be scaled down to the ratio of factor/256. When scaling down is used, the capture window explained in above has to be programmed to the corresponding size.

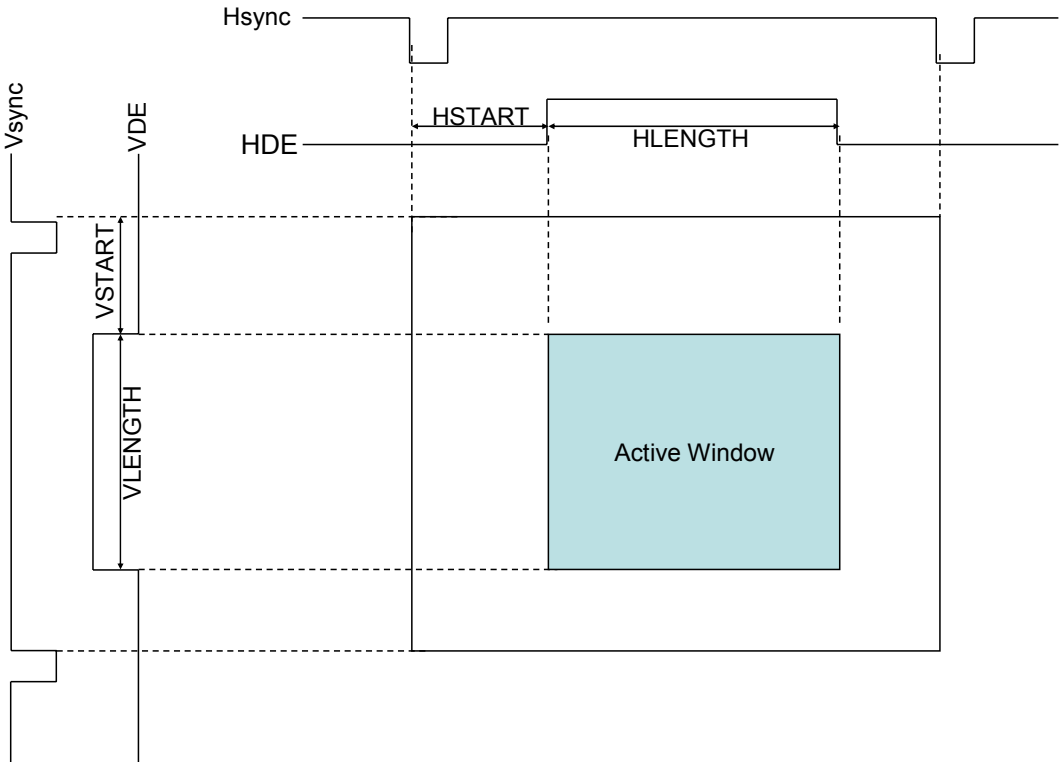


Figure 8.1.4

8.2. Audio Input Interface

The AL9V576 audio input interface is designed to work with most of the commonly available audio analog-to-digital converters (ADCs) that are compatible with the Left-Justified data format. The digitized input resolution can be 8 bits, 16 bits, or 24 bits. The audio input interface has only three pins: a left-right channel select pin (A_LEFT), an audio clock pin (A_CLK), and a serial audio data input pin (A_DATA). AL9V576 supports variable sampling rate: 32K, 44.1K, and 48K Hz.

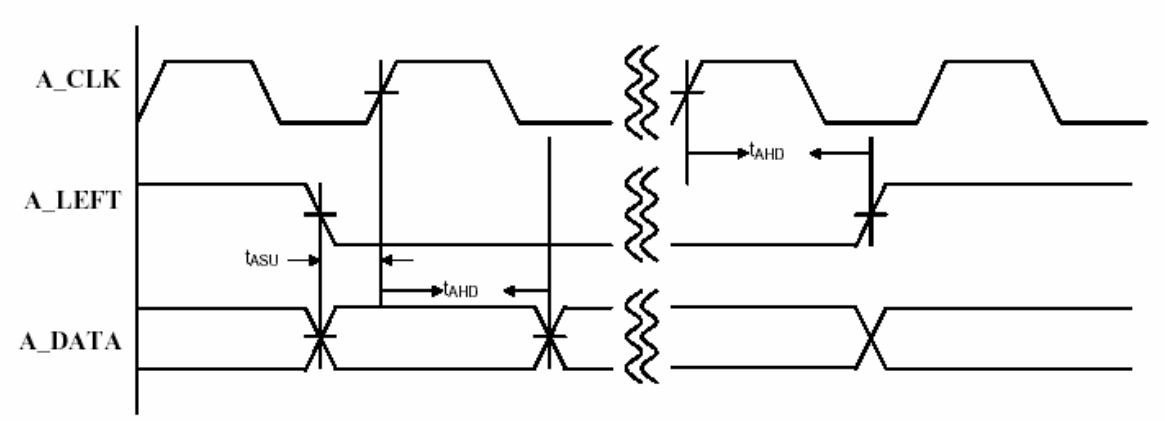


Figure 8.2.1: Audio interface timing

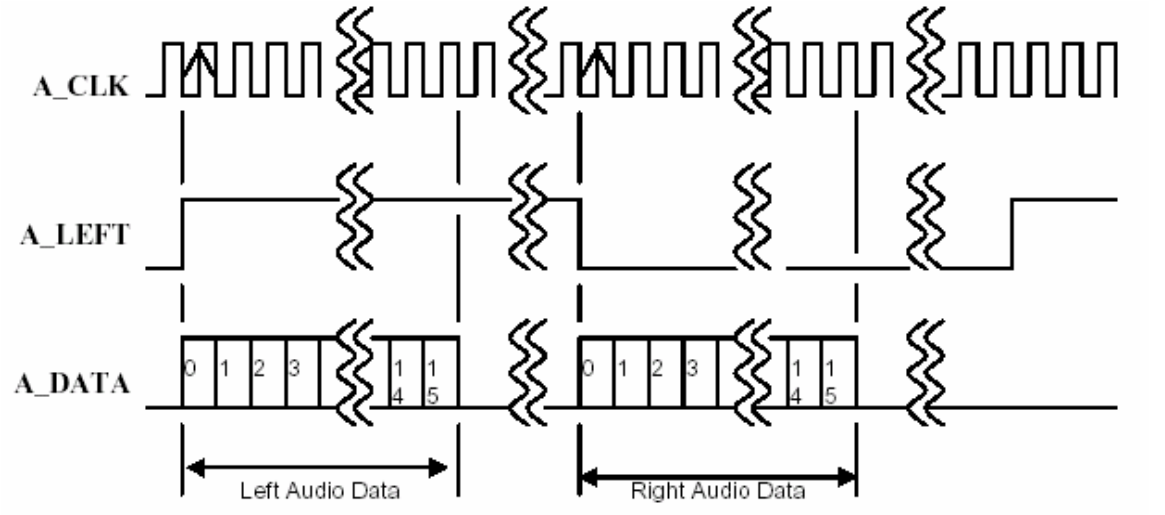


Figure 8.2.1: Left-Justified compatible timing

Table 8.2.1 Audio Timing

Symbol	Description	Min	Max	Unit
t_{ASU}	Setup time to rising of A_CLK	60	-	ns
t_{AHD}	Hold time from rising of A_CLK	60	-	ns

8.3. SDRAM Interface

AL9V576 provides a 32-bit interface to access external SDRAM. The SDRAM controller uses two-phase memory access scheme, the address/arbitration phase, and the data phase.

Interface Block Diagram

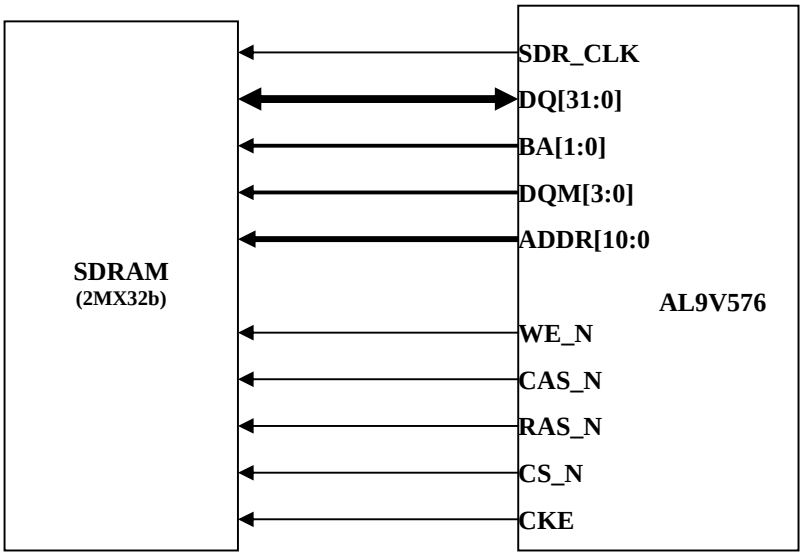


Figure 8.3.1: SDRAM Interface

Read Transaction Timing Diagram

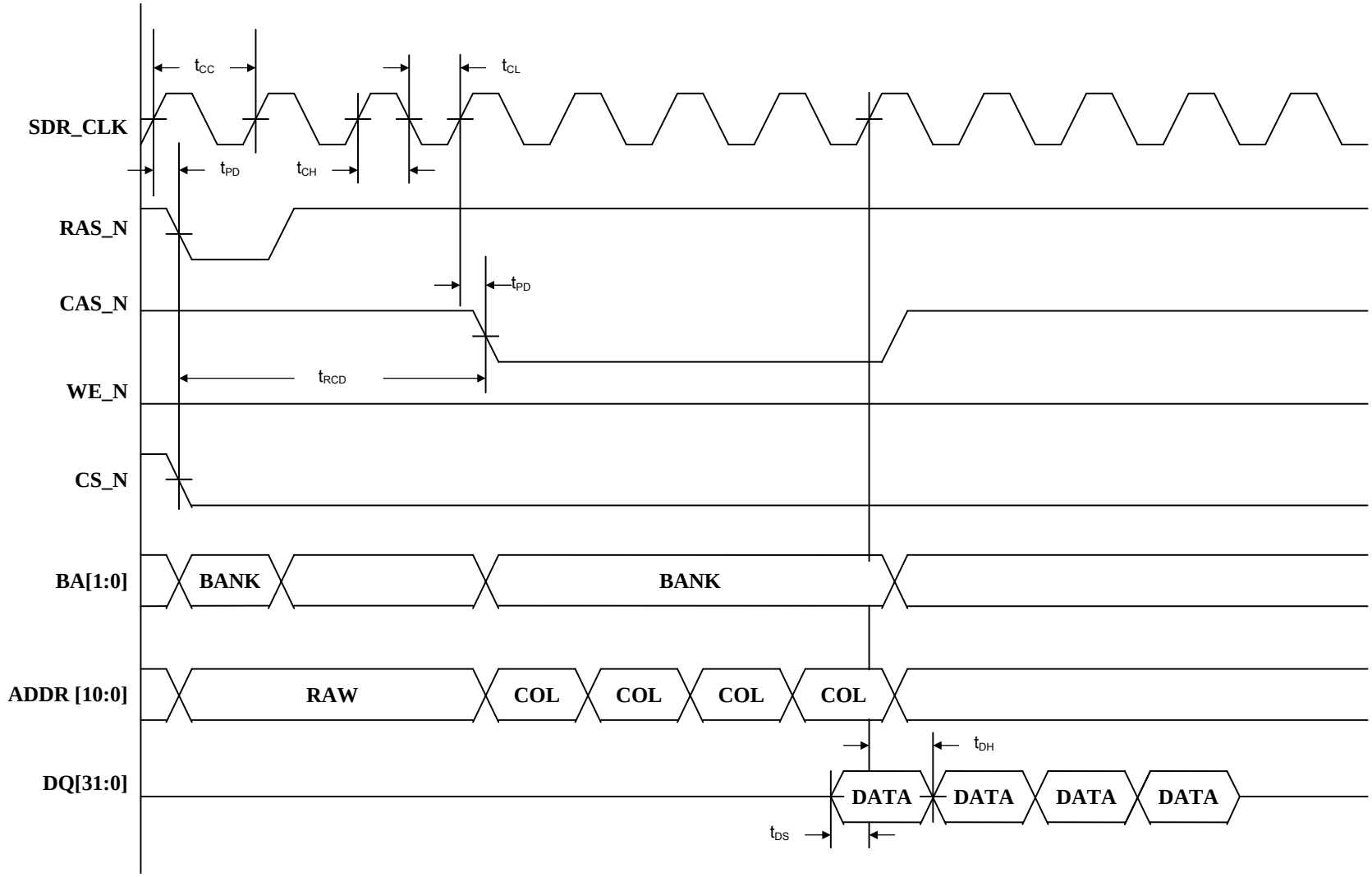


Figure 8.3.2: SDRAM Read Timing Diagram

Write Transaction Timing Diagram

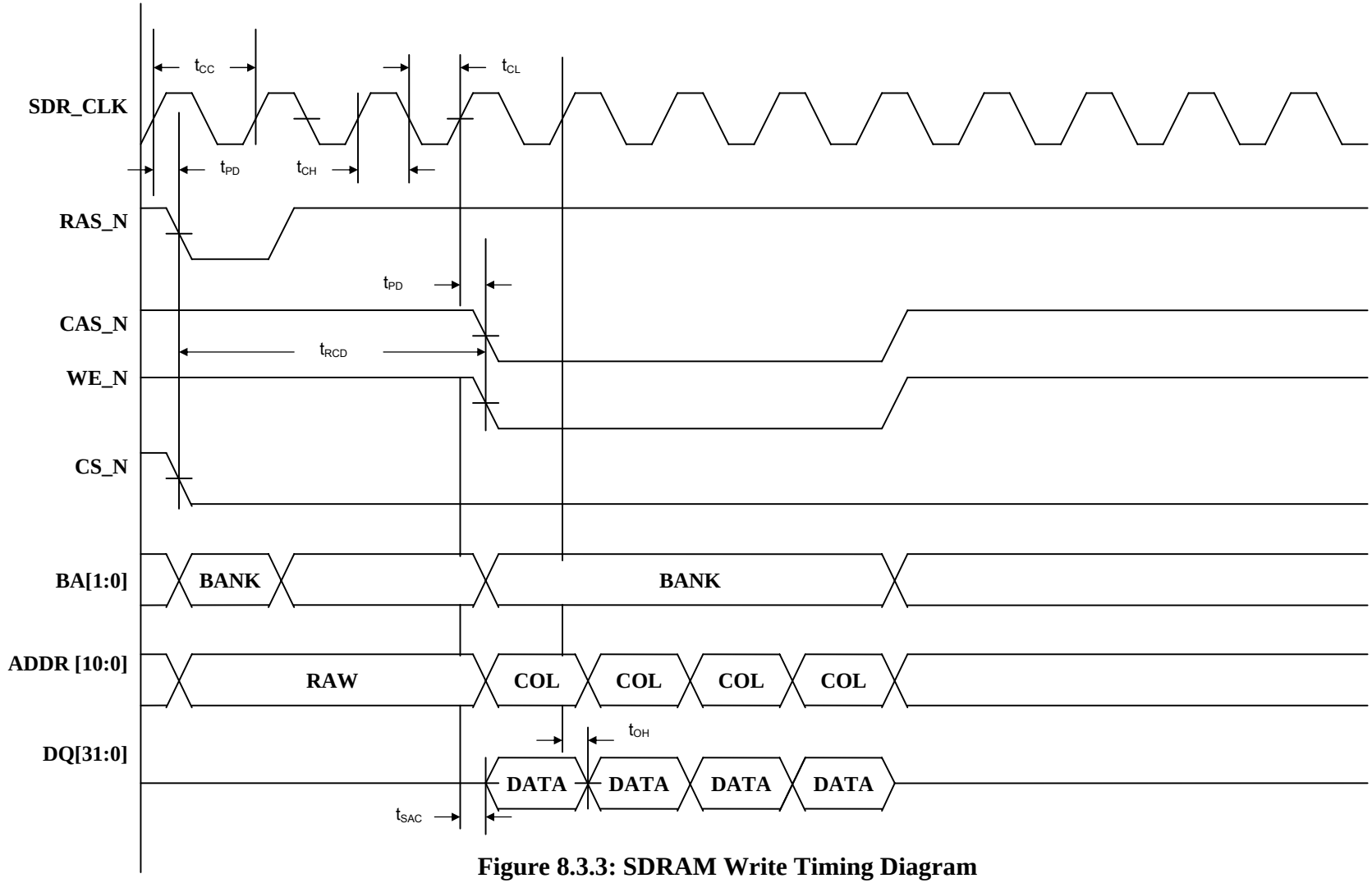


Figure 8.3.3: SDRAM Write Timing Diagram

Precharge and Refresh operation

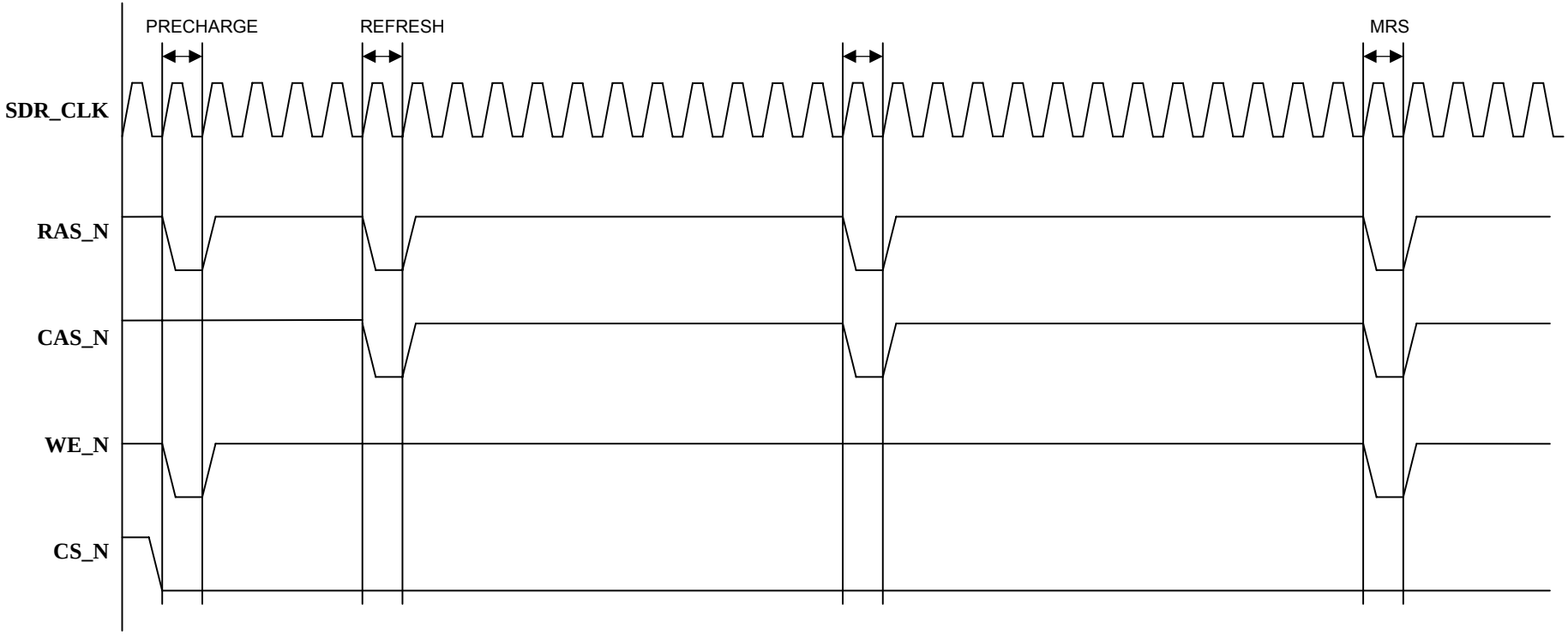


Figure 8.3.4: SDRAM Precharge and Refresh Timing Diagram

Table 8.3.1 SDRAM Timing

Symbol	Description	Min	Max	Unit
t_{CC}	SDR_CLK clock period	7.5	-	ns
t_{CH}	SDR_CLK high pulse width	3.5	-	ns
t_{CL}	SDR_CLK low pulse width	4	-	ns
t_{DS}	SDR_CLK to data input setup time	1.5	-	ns
t_{DH}	SDR_CLK to data input hold time	1	-	ns
t_{SAC}	SDR_CLK to data output delay	-	3	
t_{OH}	SDR_CLK to data output hold	3	-	
t_{PD}	SDR_CLK to (RAS_N#,CAS_N#,CS_N#,WE_N#) output delay	-	3	ns
t_{RCD}	RAS_N# to CAS_N# delay	15	-	ns

8.4. Host Interface

AL9V576 requires an external host for firmware downloading, debug access control, and compressed bit stream output. The host can be a general-purpose microcontroller or a PCI bridge connected to a PCI bus. In the case of general-purpose microcontroller, the microcontroller interface allows a host to communicate with AL9V576 through an 8-bit or a 16-bit host interface with interrupt support. AL9V576 provides two different styles of microcontroller interface, Intel-style and SRAM-style. At the top level, the two interfaces are multiplexed so that users can select one of them as the host interfaces by setting the select pin to a proper voltage level. For stand-alone applications, users can choose the 8/16-bit Intel-style or SRAM-style host interface to connect AL9V576 to a system microcontroller. In a PC-based system, the 32-bit PCI interface will be chosen to serve as the host interface.

8.4.1. PCI Interface

AL9V576 implements a PCI bus interface as an alternative of the host interface. In the current design, AL9V576 only supports target mode PCI interface that conforms to the PCI 2.2 specifications. The PCI bus interface consists of a 32-bit multiplexed address/data bus and various control signals. The host can use PCI I/O Read/Write bus commands to access the 16 HCI registers mapped onto I/O address space. Also, the host can use PCI Memory Read/Write commands to access the internal registers and memory space directly.

The timing diagrams in this section show the relationship of significant signals involved in bus transactions. When a signal is drawn as a solid line, it is actively being driven by the current master or target. When a signal is drawn as a dashed line, no agent is actively driving it. High-impedance signals are indicated to have indeterminate values when the dashed line is between the two rails.

Configuration Register Space

The PCI configuration space of any device is intended for configuration and catastrophic error-handling functions only. Access to the PCI configuration space should be limited to initialization and error-handling software. Only type 0 address formats configuration register is defined for this device.

Device ID		Vendor ID	
Status		Command	
Class Code			Revision ID
BIST	Header Type	Latency Timer	Cache Line Size
Base Address 0 (BAR0)			
Base Address 1 (BAR1)			
Base Address Registers (Reserved)			
Reserved			
Subsystem ID		Subsystem Vendor ID	
Expansion ROM Base Address			
Reserved			
Reserved			
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

Target Read Operations

A PCI read transaction starts with the address phase occurring when an initiator asserts FRAME. During the address phase, AD[31:0] contains a valid address and C/BE[3:0] contains a valid bus command. There are four types of Read operations:

- IO Read
- Direct Single Read
- Direct Burst Read
- CFG Read

Target Write Operations

A PCI write transaction starts with the address phase occurring when an initiator asserts FRAME. A write transaction is similar to a read transaction except no turnaround cycle is needed following the address phase because the initiator provides both address and data. The data phases are the same for both read and write transactions. There are four types of Read operations:

- IO Write
- Direct Single Write
- Direct Burst Write
- CFG Write

Read Transaction Timing Diagram

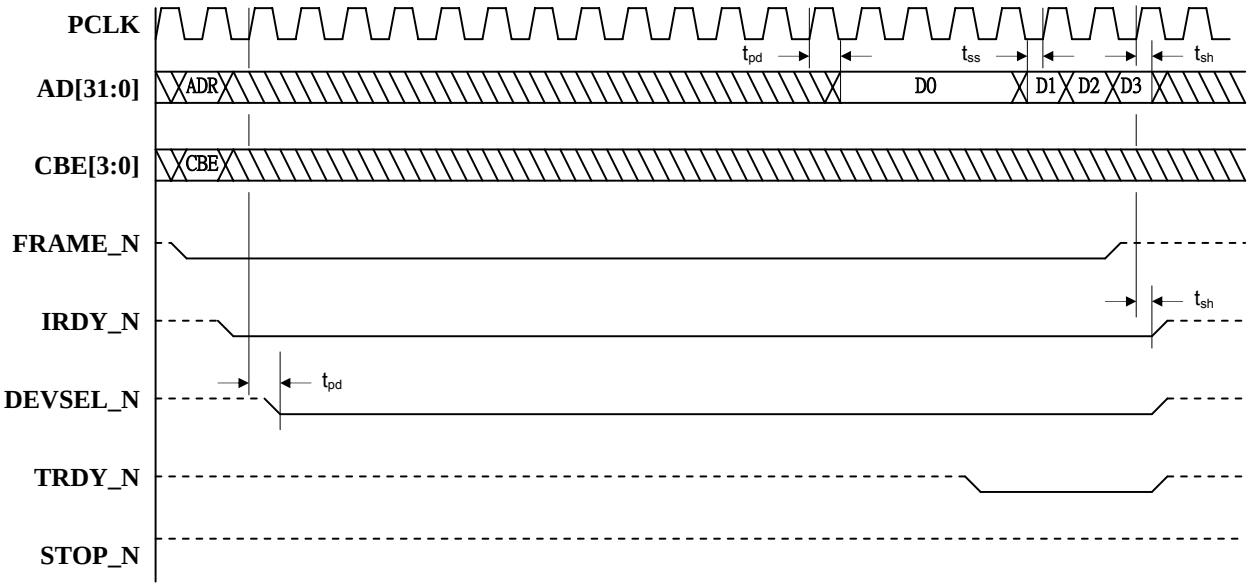


Figure 8.4.1.1: PCI Read Timing Diagram

Write Transaction Timing Diagram

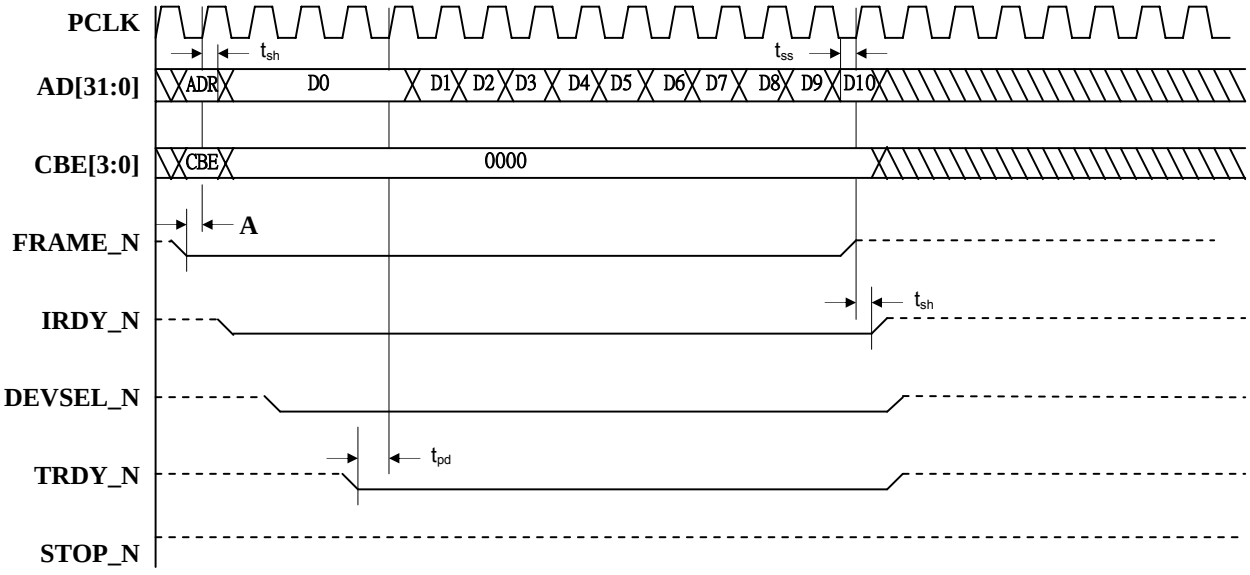


Figure 8.4.1.2: PCI write Timing Diagram

Table 8.4.1.1 PCI Timing

Symbol	Description	Min	Max	Unit
t_{pd}	Clock to output delay	-	9	ns
t_{ss}	Clock to input setup time	4	-	ns
t_{sh}	Clock to input hold time	1	-	ns

EEPROM

An external EEPROM is used to store the vendor ID and Device ID. These data will be fetched when the reset pulse is detected on the PCI local bus. The EEPROM interface consists of 3 signals, EEDI, EEDO, and EECK. The Chip Select pin should be tied to Low on the board.

Interface Block Diagram

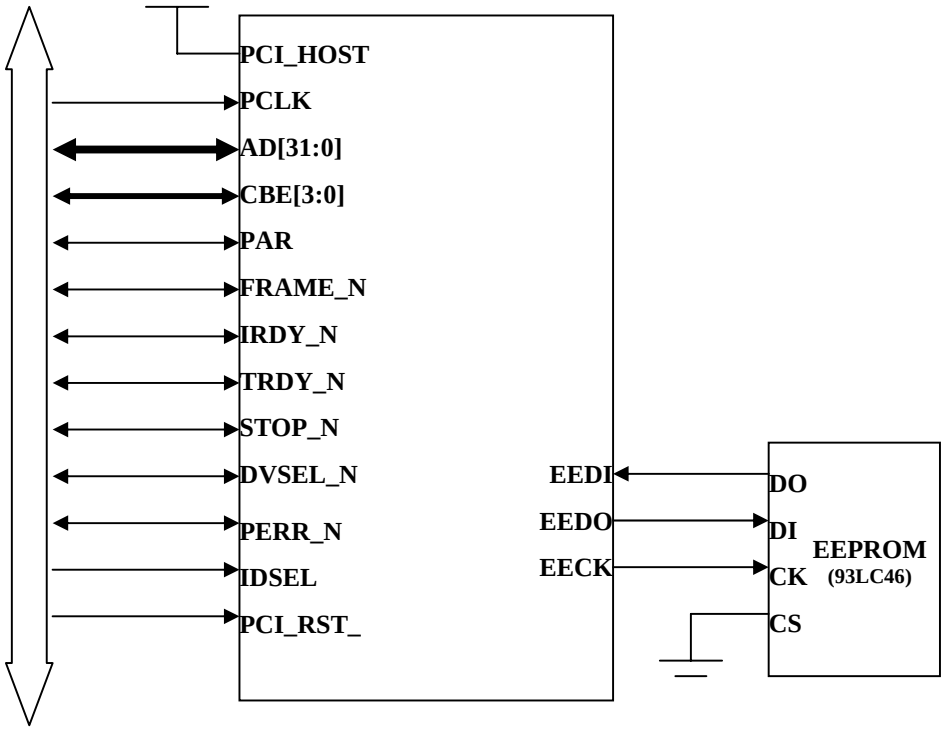


Figure 8.4.1.3: PCI Interface

8.4.2. 8/16-bit 8051 (Intel-style) Host Interface

AL9V576 provides an 8/16-bit 8051-like host interface for external registers/memory read/write operations. The interface signals are then decoded inside AL9V576 to address the registers and the memory. Please see Figure 8.4.2.1 and Figure 8.4.2.1 for the write and read operations of the Intel-style interface.

Interface Block Diagram

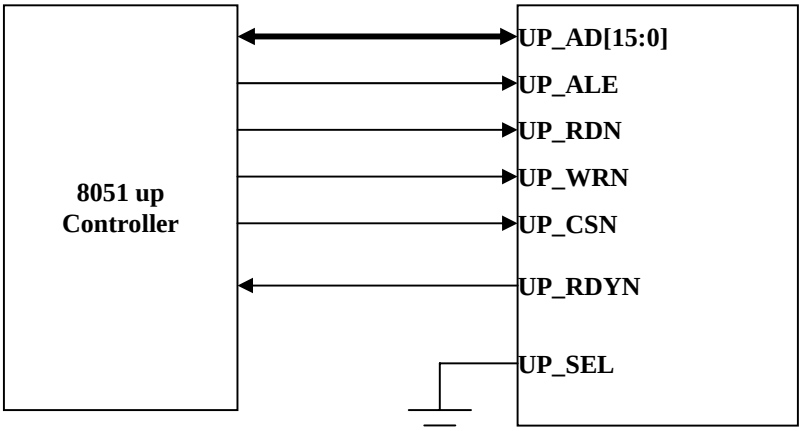


Figure 8.4.2.1: 8051 Interface

Read/Write operation and Timing Diagram

The 8051 microcontroller has to set “up_csn” to low in order to send a read/write commands to AL9V576. After “up_csn” is low, AL9V576 will latch the request address at the falling edge of “up_ale”. The read/write operation is determined using “up_rdn” and “up_wrn” signals. When “up_wrn” is low, it means the current operation is write and AL9V576 will latch in the data at the falling edge of “up_wrn”. When “up_rdn” is low and “up_wrn” is high, the host is performing read operation and AL9V576 will signal the ready of the data by setting “up_rdyn” to low.

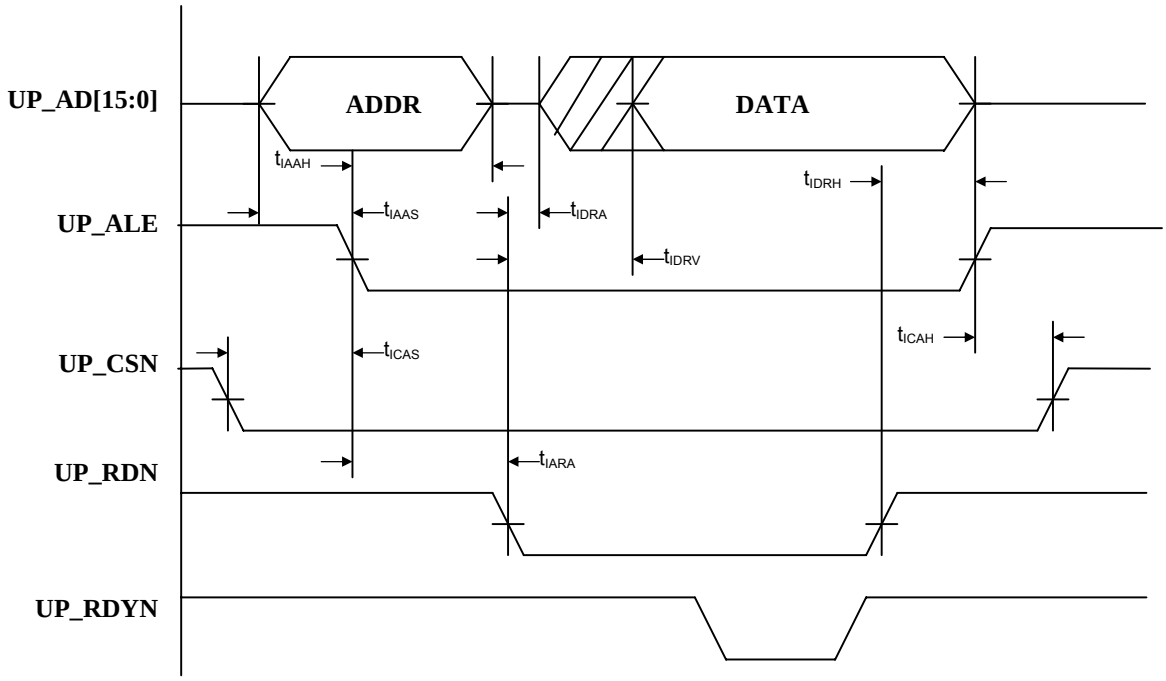


Figure 8.4.2.2: 8051 Read Transaction Timing Diagram

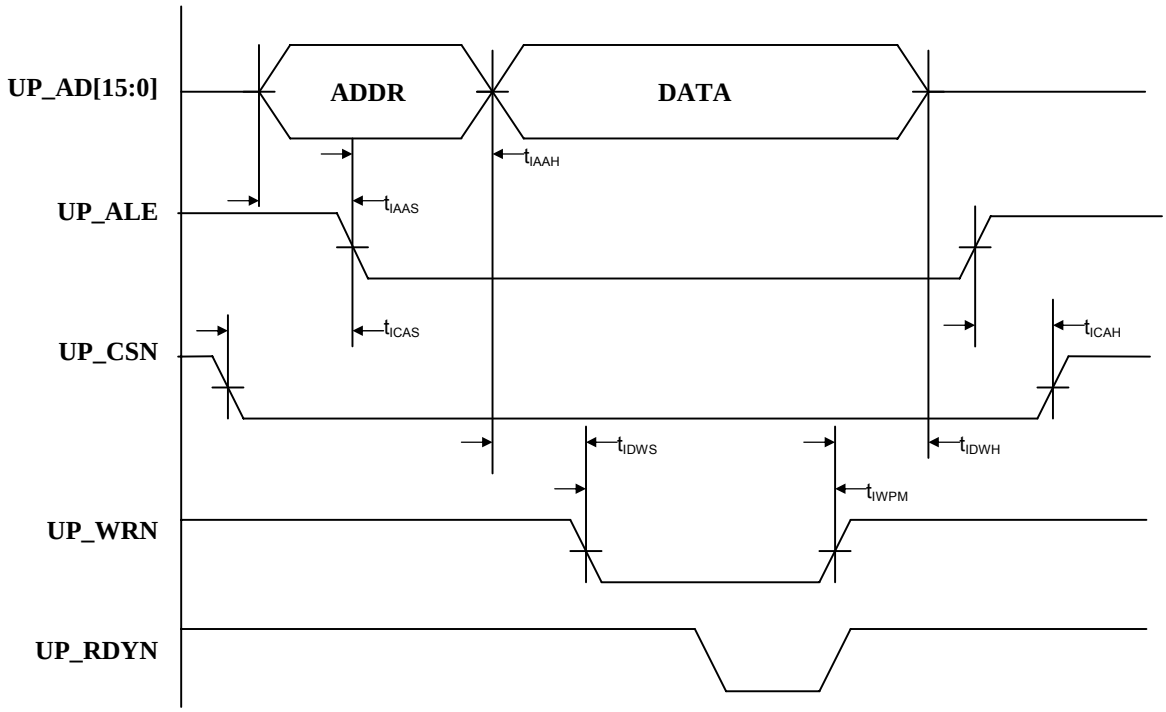


Figure 8.4.2.3: 8051 Write Transaction Timing Diagram

Table 8.4.2.1 8051 Interface Timing

Symbol	Description	Min	Max	Unit
t_{IAAS}	Address setup to falling of UP_ALE	2	-	sysCLK
t_{IAAH}	Address hold time from falling of UP_ALE	3	-	sysCLK
t_{IDRA}	Data tri-state to assertion from UP_RDN# active	2	3	sysCLK
t_{IDRV}	Data valid from beginning of UP_RDN# active	7	8	sysCLK
t_{IDRH}	Data hold from end of UP_RDN#	4	5	sysCLK
t_{ICAS}	Time from UP_CSN# active to falling of UP_ALE	2	-	sysCLK
t_{ICAH}	Time from rising of UP_ALE to UP_CSN# inactive	2	-	sysCLK
t_{IARA}	Time from falling of UP_ALE to UP_RDN# active	2	-	sysCLK
t_{IDWS}	Data valid to UP_WRN# active	2	-	sysCLK
t_{IDWH}	Data hold time from UP_WRN# inactive	2	-	sysCLK
t_{IWPM}	Minimum UP_WRN# pulse width	10	-	sysCLK
Note: sysCLK = internal system clock cycle				

8.4.3. 8/16-bit SRAM-style Microcontroller Interface

AL9V576 also provides an 8/16-bit SRAM-like host interface for external registers/memory read/write operations.

Interface Block Diagram

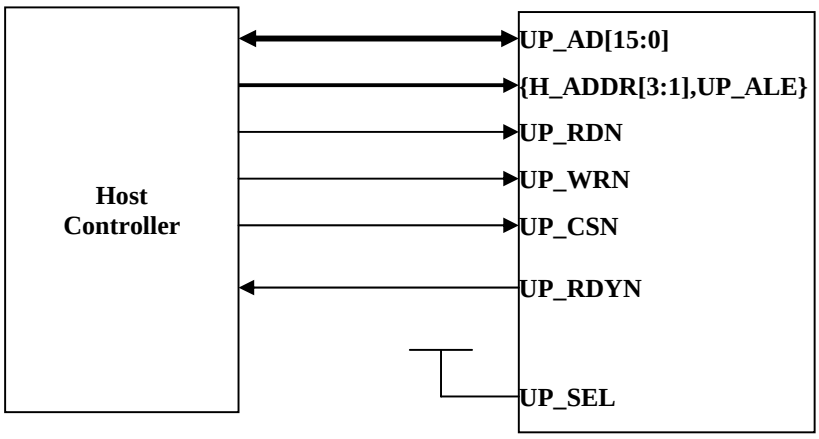


Figure 8.4.3.1: SRAM Interface

Read/Write operation and Timing Diagram

The host controller interface (HCI) consists of asynchronous signals. When writing to the HCI, the Chip Select and Write signals must be active-high and address and data must be ready for at least two HCI clocks. When read, Chip Select and Read must be active-high for at least two HCI clocks.

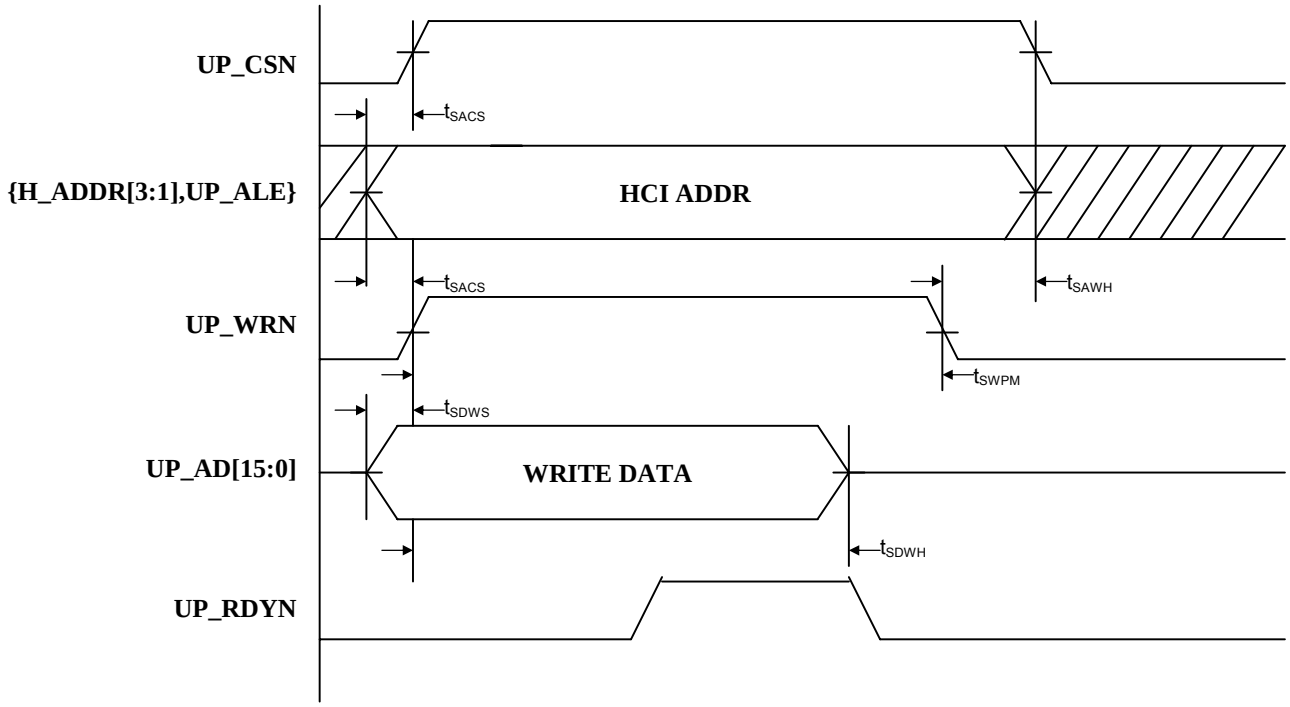


Figure 8.4.3.2: WRITE operation

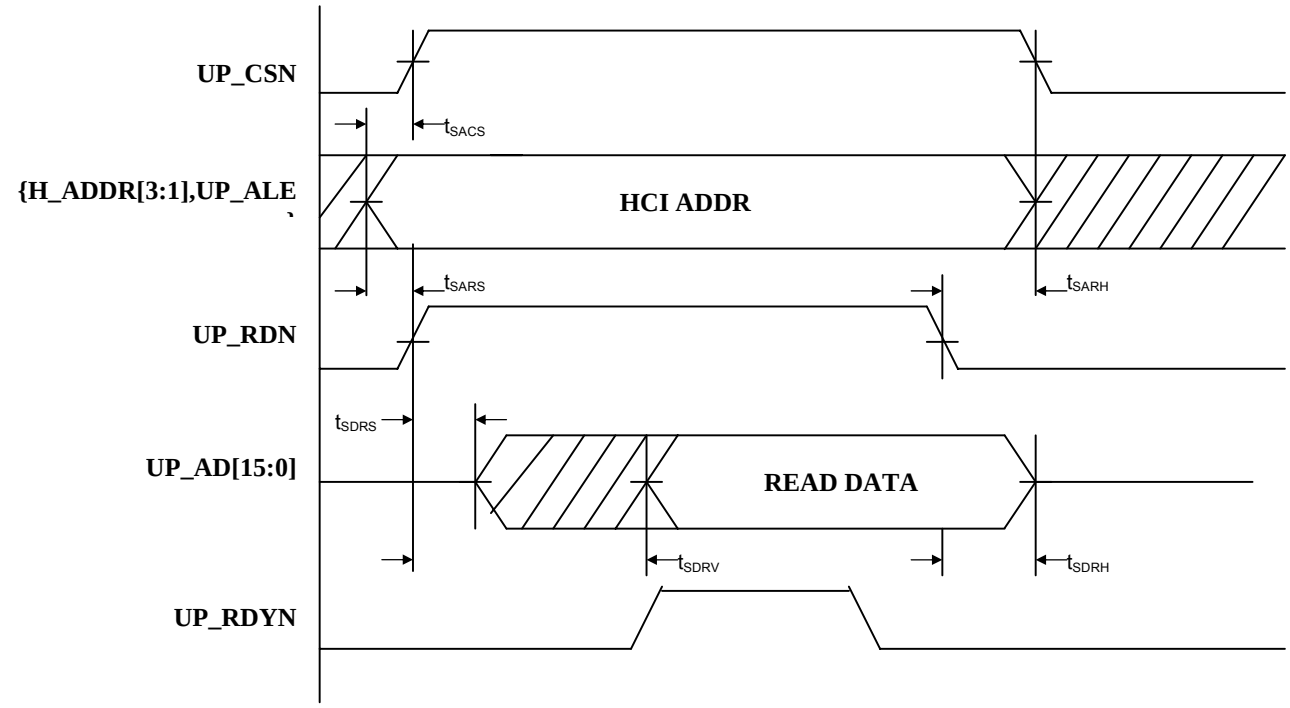


Figure 8.4.3.3: READ operation

Table 8.4.3.1 SRAM Interface Timing

Symbol	Description	Min	Max	Unit
t_{SACS}	Address setup to UP_CSN active	0	-	ns
t_{SAWS}	Address setup to UP_WRN active	0	-	ns
t_{SAWH}	Address hold from end of UP_WRN	5	-	ns
t_{SWPM}	Minimum UP_WRN active pulse width	6	-	sysCLK
t_{SDWS}	Data setup to UP_WRN active	0	-	ns
t_{SDWH}	Data hold from beginning of UP_WRN	5	-	sysCLK
t_{SARH}	Address hold from end of UP_RDN	2	-	sysCLK
t_{SDRA}	Data tri-state to assertion from beginning of UP_RDN	4	5	sysCLK
t_{SDRV}	Data valid from beginning of UP_RDN	4	5	sysCLK
t_{SDRH}	Data hold from end of UP_RDN	2	3	sysCLK
t_{SARS}	Address setup to UP_RDN active	0	-	ns
Note: sysCLK = internal system clock cycle				

8.5. System Interface

Several peripheral interfaces are designed to enhance the communication ability of AL9V576 to other components on the system. A 2-wire serial bus provides AL9V576 a simple mechanism to control general-purpose circuits such as ADC, audio/video input modules, and MPEG decoders. For encoded bit stream output, AL9V576 provides an 8-bit parallel or an 1-bit serial Encoded Stream Output (ESO) port to send the MPEG bit stream to an MPEG decoder or a wireless sender directly. There are at most 12 general-purpose IO (GPIO) ports that can receive up to 10 interrupt requests in AL9V576. These GPIO ports provide a software controlled mechanism for inter-chip communication.

8.5.1. 1/8-bit Encoded Bit Stream Output Interface

AL9V576 provides an 8-bit parallel or a 1-bit serial port for encoded bit stream output. The encoded stream output interface consists of the following signals: an 8-bit parallel (STR_DATA[7:0]) data output, a request input (STR_REQ), a data valid output (STR_DVLD), and a request clock (STR_CLK) with programmable output/input clock . The stream output FIFO size is 64 bits.

The encoded bit stream output supports handshake protocol only. To request data, the target device asserts STR_REQ when STR_DVLD is LOW. AL9V576 responds by outputting the next encoded stream data (STR_DATA), if available. The control flow of the 1-bit serial port is similar, but the serial encoded data is presented only on STR_DATA[7].

Interface Block Diagram

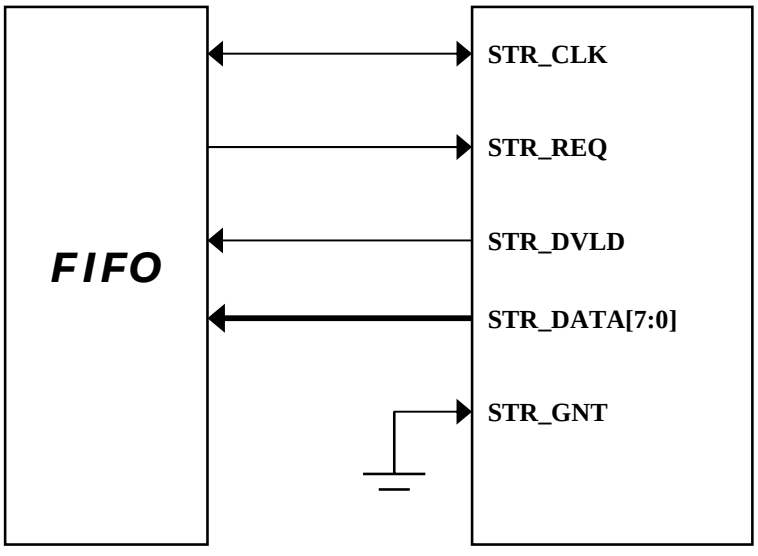


Figure 8.5.1.1: Encoded Stream Output (ESO) Interface

ESO Interface Timing Diagram

The external input pin “STR_GNT” should be pulled “LOW” to enable request pin and data bus while the ESO interface is in the process of encoded bit stream data transfer. AL9V576 supports two modes of bit stream transfer, “Program Stream Mode” and “Transport Stream Mode”. The detail timing diagrams are presented as follows:

Program Stream Mode

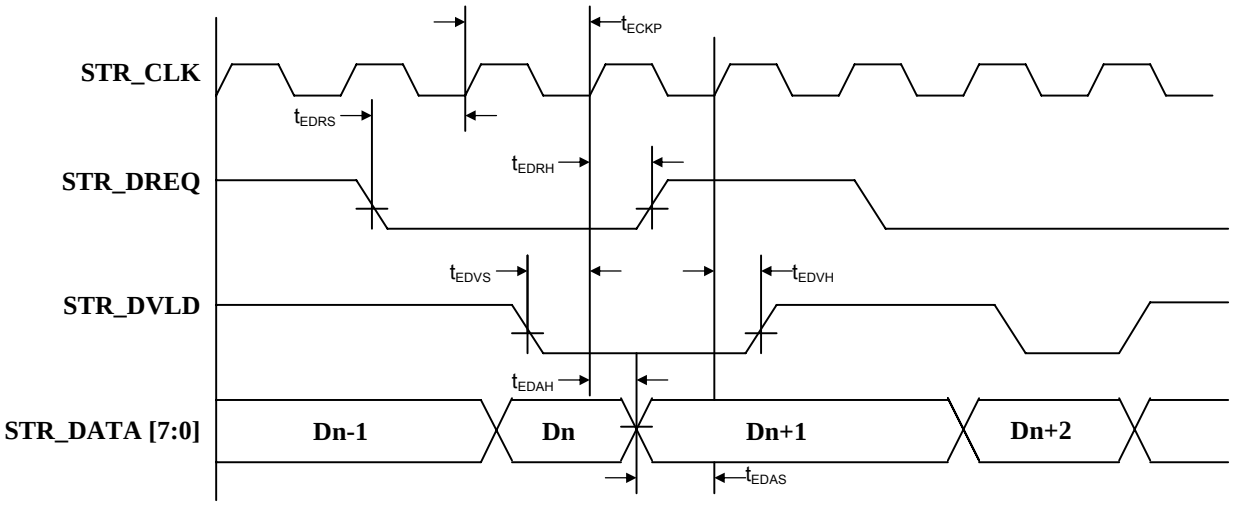


Figure 8.5.1.2: ESO Parallel Mode (PS)

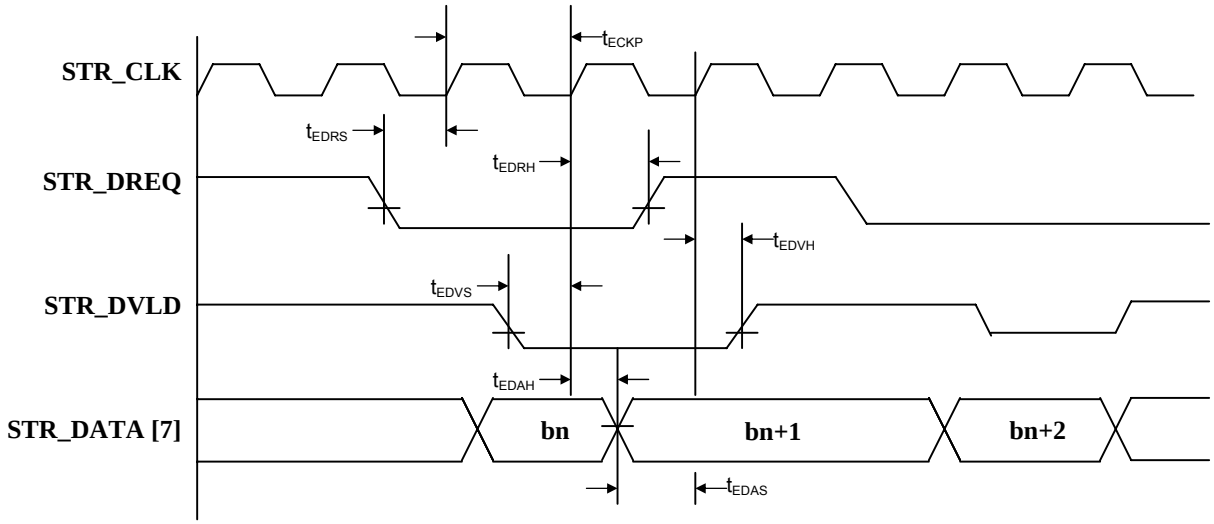
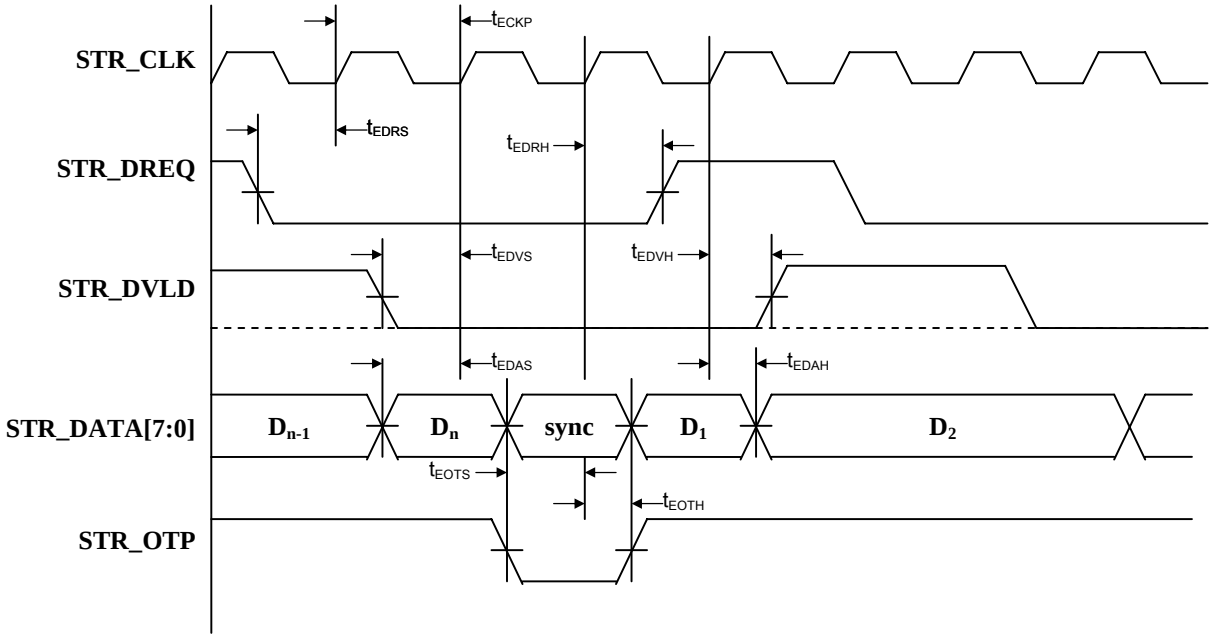


Figure 8.5.1.3: ESO Serial Mode (PS)

Transport Stream Mode



Note: STR_DLVD should be pulled **LOW** in continuous mode

Figure 8.5.1.4: ESO Parallel Mode (TS)

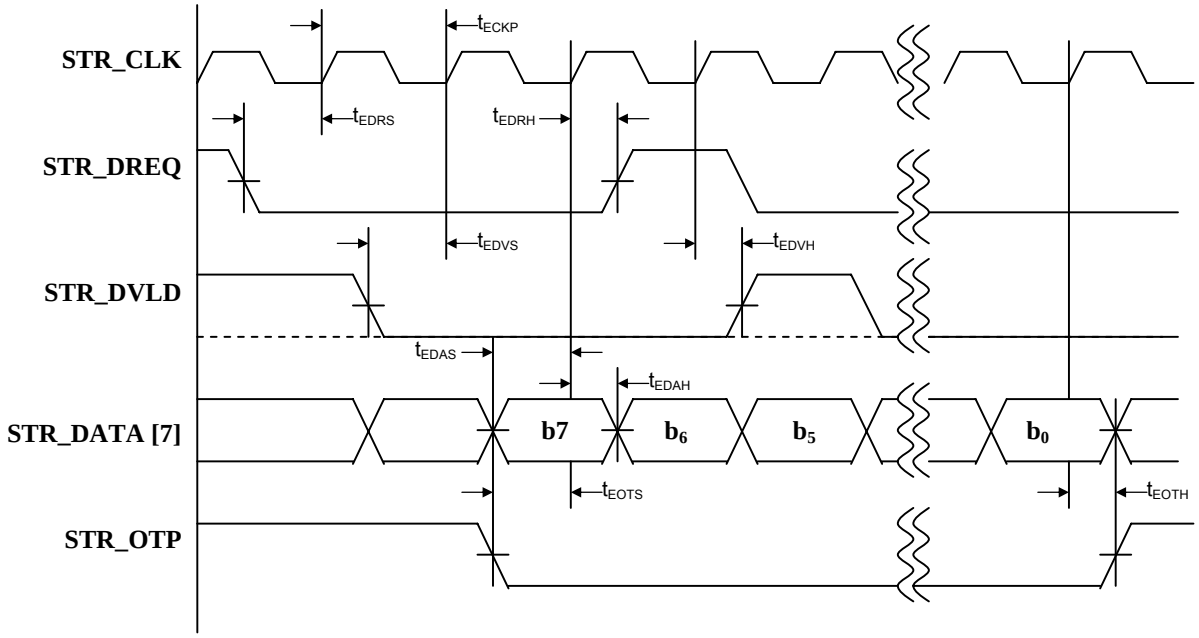


Figure 8.5.1.5: ESO Serial Mode (TS)

Symbol	Description	Min	Max	Unit
t_{ECKP}	Clock period	25	125	ns
t_{EDRS}	STR_DREQ# input setup time	5	-	ns
t_{EDRH}	STR_DREQ# input hold time	3	-	ns
t_{EDVS}	STR_DVLD# output setup time	12	-	ns
t_{EDVH}	STR_DVLD# output hold time	-	12	ns
t_{EDAH}	STR_DATA data hold time	-	10	ns
t_{EDAS}	STR_DATA data setup time	12	-	ns
t_{EOTS}	STR_OTP# output setup time	12	-	ns
t_{EOTH}	STR_OTP# output hold time	-	10	ns

ESO clock

The ESO system clock can be set as input mode or output driving mode and this setting should be fixed after power-on reset. The clock polarity can't be changed while the bit stream is being transferred to avoid the unexpected corruption of the system. For more convenient usage, AL9V576 provides four different frequencies of output clock and an option to invert clock phase for timing tuning.

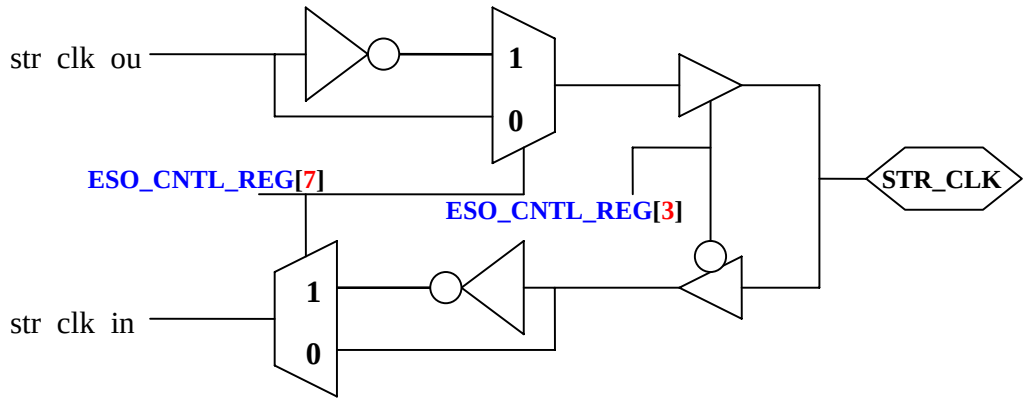


Figure 8.5.1.6: ESO Clock Selection Scheme

8.5.2. GPIO Interface

AL9V576 provides 12 user programmable general-purpose I/Os (GPIOs). They are used to implement functions that are not supported by the dedicated interface controllers in AL9V576 and require simple input/output software controlled signals.

The following lists the main features of the GPIOs:
- Most GPIOs are bi-directional and can be configured as inputs or outputs.
- GPIOs programmed as inputs can cause an interrupt request to the RISC CPU.
- All GPIOs are programmed as inputs after power-on reset.

The GPIO controller has several software accessible registers. These registers have the same bit width as the number of GPIO signals. The host can configure the type and operation of each GPIO through these registers. Table 6.1 lists the registers.

Table 8.5.2.1

Register Name	Address	Description
GPIO_OUT_MODE	0X1CD4	GPIO output data when GPIO is in output mode.
GPIO_IN_MODE	0X1CD8	GPIO input data when GPIO is in input mode.
GPIO_OE_MODE	0X1CDC	GPIO output mode setting. Active high.
GPIO_INT_MODE	0X1CE0	GPIO interrupt mode setting. "0": active high, "1": active low.

Following the power-on reset, all GPIOs are configured as input mode. All interrupts are masked so that no spurious interrupts will be generated through GPIOs. To use GPIOs as inputs only, GPIO_OE_MODE registers must remain cleared. To use GPIOs as inputs with generation of interrupts, RISC CPU has to turn off the corresponding interrupt mask. The interrupts can be configured as active-high or active-low through the programming of GPIO_INT_MODE registers. To enable the GPIO output drivers, the corresponding bit in GPIO_OE_MODE registers must be set and the corresponding interrupt mask must be turned on to disable the generation of spurious interrupts.

8.5.3. 2-Wire Serial Bus (I^2C-like) Interface

The serial bus is a simple 2-wire bi-directional bus for efficient inter-IC control. The following lists the important features of the serial (I^2C-like) bus:

- Only two bus lines are required; a serial data line SDA and a serial clock line SCL.
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times. A master can operate as a master-transmitter or as a master-receiver.
- It is a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer.
- Serial, 8-bit oriented, bi-directional data transfers can be made up at up to 100 K bits/s in the Standard-mode, up to 400 K bits/s in the Fast-mode, or up to 3.4 M bits/s in the High-speed mode.
- On-chip filtering rejects spikes on the bus data line to preserve data integrity.
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

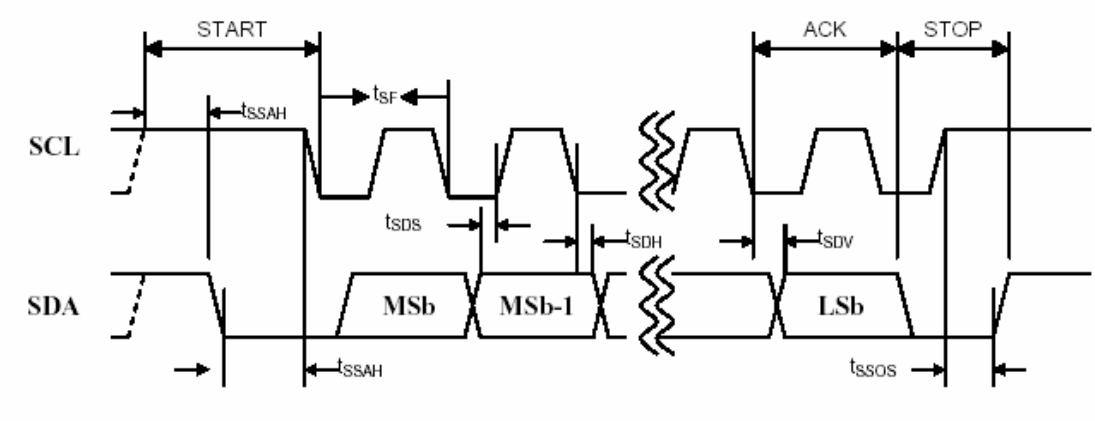


Figure 8.5.3.1: Data transfer on the 2-wire serial bus

Symbol	Description	Min	Max	Unit
t_{SSAH}	The hold time of START condition	112	-	ns
t_{SDS}	SDA setup time	112	-	ns
t_{SDH}	SDA hold time	127	-	ns
t_{SDV}	SDA output valid from the low of SCL	-	240	ns
t_{SSOS}	The setup time of STOP condition	210	-	ns
t_{SF}	SCL frequency	-	1.5	MHz

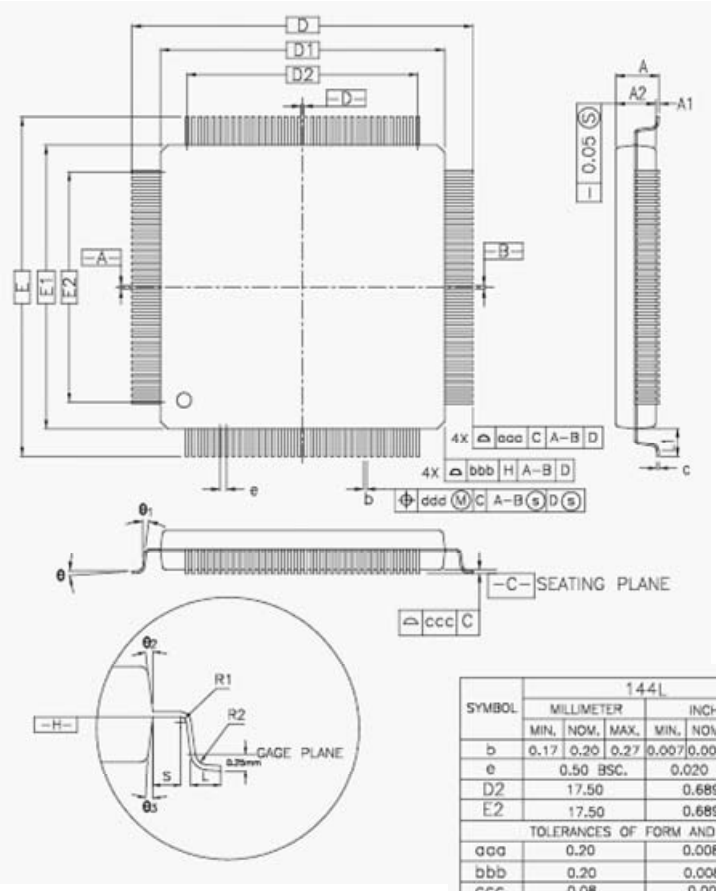
Figure 8.5.3.1 illustrates the data transfer on the 2-wire serial bus. Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is

unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

The 2-wire serial bus controller of AL9V576 supports single-master mode only. This means only AL9V576 is capable of controlling the bus. The 2-wire serial bus controller is programmed through the local register access. Either the RISC processor or the host microcontroller can initiate 2-wire serial bus transfer.

9. Mechanical Dimension

160 Pin LQFP 20mm x 20mm x 1.4mm

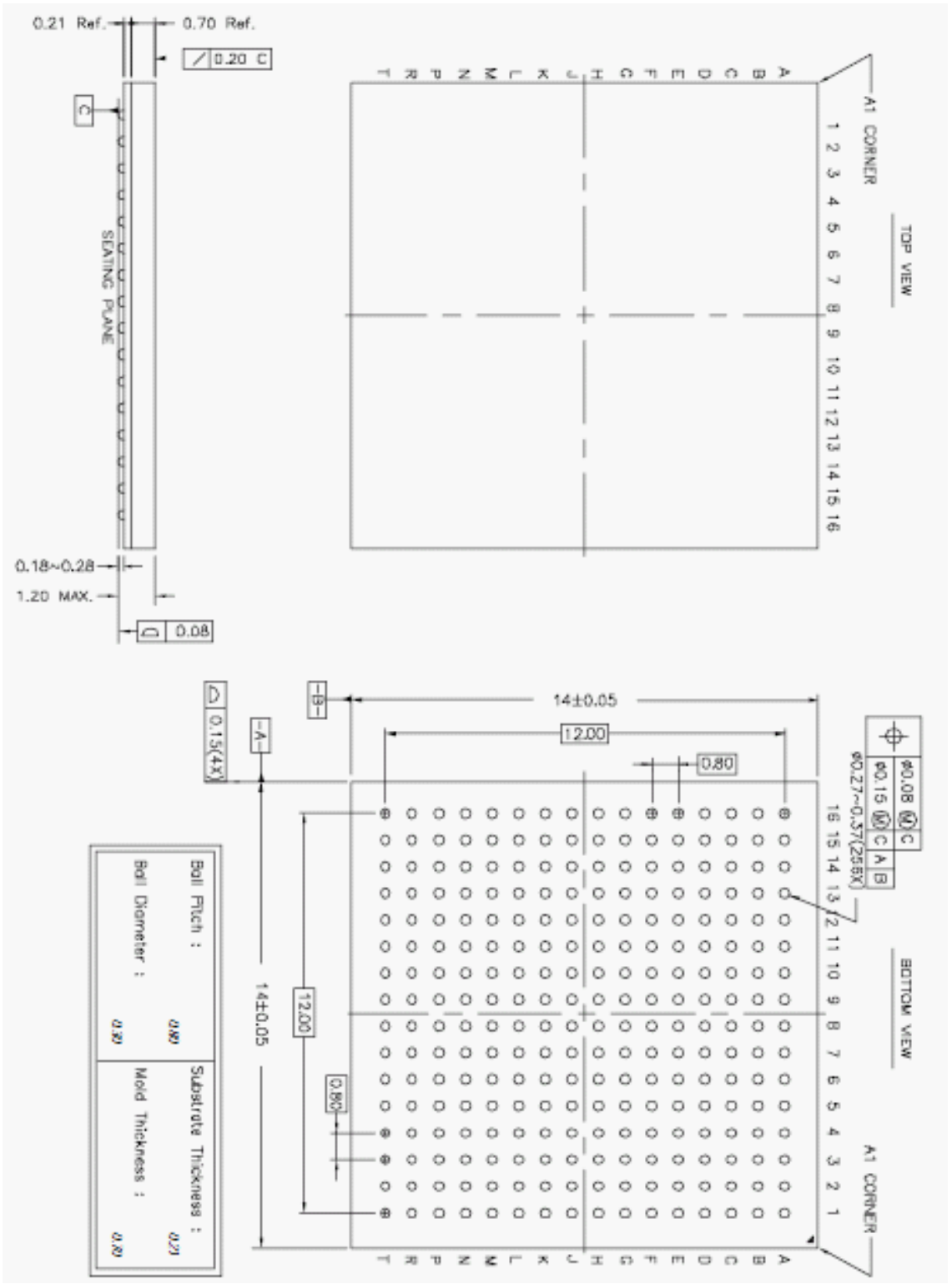


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	22.00 BSC.			0.866 BSC.		
E1	20.00 BSC.			0.787 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	144L						160L						176L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011	0.13	0.16	0.23	0.005	0.006	0.009	0.13	0.16	0.23	0.005	0.006	0.009
e	0.50 BSC.			0.020 BSC.			0.40 BSC.			0.016 BSC.			0.40 BSC.			0.016 BSC.		
D2	17.50			0.689			15.60			0.614			17.20			0.677		
E2	17.50			0.689			15.60			0.614			17.20			0.677		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.08			0.003			0.08			0.003			0.08			0.003		
ddd	0.08			0.003			0.07			0.003			0.07			0.003		

256 Pin TfBGA 14mm x 14mm x 1.2mm



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